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PATENT ABSTRACTS OF JAPAN

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(54) FIELD-EFFECT TRANSISTOR AND MANUFACTURE THEREOF, SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF AND LOGIC CIRCUIT CONTAINING SEMICONDUCTOR DEVICE THEREOF AND SEMICONDUCTOR SUBSTRATE

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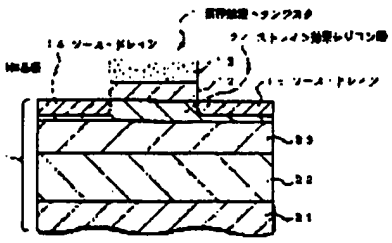

(57)Abstract:
PROBLEM TO BE SOLVED: To improve the performance of a transistor by increasing the mobility of the transistor while preventing the generation of junction leakage.
SOLUTION: When a transistor 1 is formed to a strain-effect silicon layer 24 of a semiconductor layer having a strain effect formed to the upper layer of a semiconductor substrate 11, a source and a drain 14, 15 shaped only to the strain-effect silicon layer 24. The transistor 1 is formed as an N channel MOS transistor, and a P channel MOS transistor can also be formed to the strain-effect silicon layer 24 through an element isolation region. The logic circuit can also be constituted of these transistors.

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CLAIMS

[Claim(s)]

[Claim 1] the field-effect transistor which is a field-effect transistor formed in the semiconductor layer which has the strain effect currently formed in the semiconductor substrate upper layer, and is characterized by forming the source drain of the aforementioned field-effect transistor only in the half-conductor layer which has the aforementioned strain effect

[Claim 2] The semiconductor layer which has the aforementioned strain effect in a field-effect transistor according to claim 1 is a field-effect transistor characterized by the bird clapper from the silicon layer which has the strain effect.

[Claim 3] The field-effect transistor characterized by having the silicon epitaxial layer formed on the aforementioned source drain, and the refractory-metal silicide layer formed in the aforementioned silicon epitaxial layer in a field-effect transistor according to claim 2.

[Claim 4] It is the field-effect transistor which characterizes by the bird clapper from the buffer layer which consists of the silicon germanium from which it is what that formed the aforementioned semiconductor substrate on a silicon substrate and the aforementioned silicon substrate in a field-effect transistor according to claim 2, and germanium concentration changes in the thickness direction, the relaxed layer which consist of the silicon germanium with which it is what that formed on the aforementioned buffer layer, and stress is eased, and the silicon layer which have the strain effect which formed on an aforementioned relaxed layer.

[Claim 5] It is the field-effect transistor which characterizes by the bird clapper from the buffer layer which consists of the silicon germanium from which it is what that formed the aforementioned semiconductor substrate on a silicon substrate and the aforementioned silicon substrate in a field-effect transistor according to claim 3, and germanium concentration changes in the thickness direction, the relaxed layer which consist of the silicon germanium with which it is what that formed on the aforementioned buffer layer, and stress is eased, and the silicon layer which have the strain effect which formed on an aforementioned relaxed layer.

[Claim 6] The manufacture method of a field-effect transistor characterized by providing the following. The process which forms the semiconductor layer which has the strain effect it is ineffective in the upper layer of a semiconductor substrate, and constitutes this semiconductor substrate. The process which forms a gate electrode through a gate insulator layer on the semiconductor layer which has the aforementioned strain effect. the process which dopes the impurity for forming a source drain in the semiconductor layer which has the aforementioned strain effect in the both sides of the aforementioned gate electrode and which forms a source drain especially therefore

[Claim 7] The manufacture method of the field-effect transistor characterized by forming the semiconductor layer which has the aforementioned strain effect in the manufacture method of a field-effect transistor according to claim 6 in the silicon layer which has the strain effect.

[Claim 8] The manufacture method of the field-effect transistor characterized by performing the process which forms a silicon epitaxial layer on this source drain, and the process which forms a refractory-metal silicide layer in the aforementioned silicon epitaxial layer in the manufacture method of a field-effect transistor according to claim 7 after forming the aforementioned source drain.

[Claim 9] the semiconductor device which is a semiconductor device which consists of a p-channel type field-effect transistor formed in the semiconductor layer which has the strain effect currently formed in the semiconductor substrate upper layer, and an n channel type field-effect transistor, and is characterized by forming the source drain of the aforementioned p-channel type field-effect transistor, and the source drain of an n channel type field-effect transistor only in the half-conductor layer which has the aforementioned strain effect

[Claim 10] The s miconductor layer which has the aforementioned strain effect in a semiconductor device according to claim 9 is a semiconductor device characterized by the bird clapper from the silicon layer which has the strain effect.

[Claim 11] The semiconductor device characterized by having the silicon epitaxial layer formed on each aforementioned source drain, and the refractory-metal silicide lay r formed in the aforementioned silicon epitaxial layer in a semiconductor device according to claim 10.

[Claim 12] The semiconductor device according to claim 10 characterized by providing the following. The aforementioned semiconductor substrate is a silicon substrate. The buffer layer which consists of silicon germanium from which it is what was formed on the aforem ntioned silicon substrate, and germanium concentration was changed in the thickness direction. The relaxed layer which consists of silicon germanium with which it is what was formed on the aforementioned buffer layer, and stress is eased. The silicon layer which has the strain effect formed on the aforementioned relaxed layer.
[Claim 13] The semiconductor device according to claim 11 characterized by providing the following. The aforementioned semiconductor substrate is a silicon substrate. The buffer layer which consists of silicon germanium from which it is what was formed on the aforementioned silicon substrate, and germanium concentration was changed in the thickness direction. The relaxed layer which consists of silicon germanium with which it is what was formed on the aforementioned buffer layer, and stress is eased. The silicon layer which has the strain effect formed on the aforementioned relaxed layer.
[Claim 14] The manufacture method of a semiconductor device characterized by providing the following. The process which forms the silicon layer which has the strain effect it is ineffective in the upper layer of a semiconductor substrate, and constitutes this semiconductor substrate. The process which forms the gate electrode of a p-channel type field-effect transistor, and the gate electrode of an n channel type field-effect transistor through a gate insulator layer on the silicon layer which has the aforementioned strain effect. The process which forms the source drain which becomes the silicon layer which has the aforementioned strain effect in the both sides of the gate electrode of the aforementioned p-channel type field-effect transistor from p type diffusion layer. The process which forms the source drain which becomes the silicon layer which has the aforementioned strain effect in the both sides of the gate electrode of the aforementioned n channel type field-effect transistor from n type diffusion layer.
[Claim 15] The manufacture method of the semiconductor device characterized by performing the process which forms a silicon epitaxial layer on each of this source drain, and the process which forms a refractory-metal silicide layer in the aforementioned silicon epitaxial layer in the manufacture method of a semiconductor device according to claim 14 after forming each aforementioned source drain.
[Claim 16] In the logical circuit containing the semiconductor device equipped with the p-channel type field-effect transistor and the n channel type field-effect transistor, the semiconductor substrate which forms this logical circuit While consisting of a semiconductor substrate by which the silicon layer which has the strain effect is formed in the upper layer and forming the source drain of the aforementioned p-channel type field-effect transistor only in the silicon layer which has the aforementioned strain effect The source drain of the aforementioned n channel type field-effect transistor is a logical circuit containing the semiconductor device characterized by being formed only in the silicon layer which has the aforementioned strain effect.
[Claim 17] The semiconductor substrate characterized by the bird clapper from a germanium substrate, the relaxed layer which consists of a silicon germanium layer which is what was formed on the aforementioned germanium substrate, and by which stress is eased, and the silicon layer which has the strain effect formed on the aforementioned relaxed layer.
[Claim 18] It is the field-effect transistor characterized by the bird clapper from the relaxed layer which consists of a silicon germanium layer which is what formed the aforementioned semiconductor substrate on the germanium substrate and the aforementioned germanium substrate in the field-effect transistor according to claim 2, and by which stress is eased, and the silicon layer which has the strain effect formed on the aforementioned relaxed layer.
[Claim 19] It is the field-effect transistor characterized by the bird clapper from the relaxed layer which consists of a silicon germanium layer which is what formed the aforementioned semiconductor substrate on the germanium substrate and the aforementioned germanium substrate in the field-effect transistor according to claim 3, and by which stress is eased, and the silicon layer which has the strain effect formed on the aforementioned relaxed layer.
[Claim 20] It is the semiconductor device characterized by the bird clapper from the relaxed layer which consists of a silicon germanium layer which is what formed the aforementioned semiconductor substrate on the germanium substrate and the aforementioned germanium substrate in the semiconductor device according to claim 10, and by which stress is eased, and the silicon layer which

has the strain effect formed on the aforementioned relaxed lay r.
[Claim 21] It is the semiconductor device characterized by th bird clapper from the relaxed layer which consists of a silicon germanium layer which is what formed the aforementioned semiconductor substrate on the germanium substrate and the aforementioned germanium substrate in th semiconductor device according to claim 11, and by which stress is eased, and the silicon layer which has the strain effect formed on the aforementioned relaxed layer.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention relates to the semiconductor substrate in which the logical circuit and they which contain the field-effect transistor in_which the source drain was formed, the semiconductor device containing the manufacture method and its field-effect transistor, and the manufacture method and its semiconductor device in the silicon layer which has the strain effect in detail are formed about the logical circuit and the semiconductor substrate containing a field-effect transistor, the manufacture method and a semiconductor device, and the manufacture method and its semiconductor device.
[0002]
[Description of the Prior Art] The device by the material using the strain (distortion) effect is becoming possible by progress of IV group semiconductor materials, such as silicon / silicon germanium, and a thin film coating technology, and the research which aimed at high efficiency and the low-battery device is very prosperous in it now. In a thin film semiconductor, an energy band is distorted and the above-mentioned strain effect means that the effective mass of a carrier changes, when a film receives stress. it is becoming possible to form the semiconductor thin film which has this strain effect by devising multilayers, such as for example, silicon / silicon germanium, and controlling membranous internal stress by molecular beam epitaxy technology, chemical vapor-growth (UHV-CVD) technology under an ultra-high vacuum, etc. Thus, development of a highly efficient MOS system device, a sensor, etc. is also progressing by controlling a band-gap difference and a membranous strain by the heterojunction.
[0003] In the case of a silicon film, tensile stress will be received by the silicon film of the SOI (Silicon on insulator) substrate formed by the formation technology of a zone melt method and the single-crystal-silicon film by irradiation of an Ar ion laser etc. On the other hand, compressive stress will be received by the silicon film of an SOS (Silicon on Sapphire) substrate. Consequently, in the former, the degree of electron transfer becomes large, and the mobility of an electron hole becomes large in the latter. In other words, in the former, the mobility of an electron hole becomes small, and the degree of electron transfer becomes small by the latter.
[0004] Moreover, if depositing a silicon film on the epitaxial layer of the so-called silicon germanium in the relaxed state where stress is eased in the case of a silicon system MOS (Metal-Oxide-Semiconductor) transistor, speaking concretely, improvement in the degree of electron transfer can b aimed at with tensile stress (if it says strictly, the band which degenerated to six is explained to be divided into two bands with which effective masses differ). On the other hand, if the silicon germanium (so-called germanium rich silicon germanium) film containing many germanium is formed, improvement in the mobility of an electron hole can be aimed at with compressive stress.
[0005] Based on the property of such a strain effect silicon layer, the result of a high mutual conductance [gm (mobility)] is obtained by the MOS transistor which controlled and produced the stress of the layer which forms a multilayer and serves as a channel. Appl.Phys.Letter (USA), 63 (1993) S.P.Voinigensen et al., and p660 And IEEE Electronic Devices (USA), 43 (1996) L.H.Jiang and R.G.Elliman, and p97 **** -- the pMOS transistor is indicated Moreover, Appl.Phys.Lett r (USA), 64 (1994) Klsmail et al., and p3124 (1994) And the nMOS transistor is indicated by IEDM 94-37 (USA) and J.Welser et al.

[0006] On the other hand, the path transistor is proposed as lat st highly efficient logic (LOGIC) which performs low-battery operation, and the proposal in the latest applied-technology fields, such as CPU (Central Processig Unit) and MPEG (Moving Picture Experts Group), is made. Such a logical circuit requires the highly efficient prop rty that the nMOS transistor used as a subject has a high mutual conductance in low-battery operation. On the other hand, even if there are few element numbers at precharge usage [a pMOS transistor] etc., a demand is not carried out but the working speed like a nMOS transistor determines a performance by adjustment of channel width W, it is not disadvantageous in area.

[0007]

[Problem(s) to be Solved by the Invention] however, with the pMOS transistor and nMOS transistor in a Prior art which gave [above-mentioned] explanation, since junction of a source drain is located in the small silicon germanium layer of a band gap when application by the highly efficient low battery is considered, and since junction of a source drain is formed in silicon / silicon germanium interface, the xistence which is leak serves as a technical problem

[0008]

[Means for Solving the Problem] this invention is a semiconductor substrate at the logical circuit row containing the field-effect transistor made in order to solve the above-mentioned technical problem and its manufacture method, a semiconductor device and its manufacture method, and its semiconductor device.

[0009] a field-effect transistor is formed in the silicon layer (henceforth the strain effect silicon layer) which is a semiconductor layer which has the strain effect currently formed in the semiconductor substrate upper layer, and the source drain of this field-effect transistor is formed in the strain effect silicon layer chisel

[0010] In the above-mentioned field-effect transistor, since the source drain is formed only in the strain effect silicon layer, junction of a source drain will exist in the strain effect silicon layer. Therefore, generating of junction leak stops being able to occur easily.

[0011] The manufacture method of a field-effect transistor forms the silicon layer (the strain effect silicon layer) which is a semiconductor layer which has the strain effect it is ineffective in the upper layer of a semiconductor substrate, and constitutes this semiconductor substrate. Then, a gate electrode is formed through a gate insulator layer on the strain effect silicon layer. And it is the manufacture method equipped with the process of forming a source drain, by doping the impurity for forming a source drain in the silicon layer which has the strain effect in the both sides of a gate el ctrode.

[0012] By the manufacture method of the above-mentioned field-effect transistor, since the source drain of a field-effect transistor is formed only in the strain effect silicon layer, junction of a source drain will be formed only in the strain effect silicon layer. Therefore, generating of junction leak is suppressed.

[0013] the p-channel type field-effect transistor and n channel type field-effect transistor which were formed in the silicon layer (the strain effect silicon layer) which is a semiconductor layer which has the strain effect currently formed on the semiconductor substrate including a field-effect transistor in which the semiconductor device gave [above-mentioned] explanation -- since -- it becomes and each source drain of a p-channel type and an n channel type field-effect transistor is formed only in the strain effect silicon layer

[0014] In the above-mentioned semiconductor device, since each source drain of a p-channel type and an n channel type field-effect transistor is formed only in the strain effect silicon layer, junction of each source drain will exist in the strain effect silicon layer. Therefore, it is hard coming to generate junction leak. Moreover, it becomes the conventional CMOS structure and almost equivalent structure from each source drain being formed in the one strain effect silicon layer. Therefore, structure becomes easy.

[0015] The manufacture method of a semiconductor device forms the strain effect silicon layer used as the upper layer of a semiconductor substrate, and constitutes this semiconductor substrat . The gat electrode of a p-channel type field-effect transistor and the gate electrode of an n channel type field-effect transistor are formed through a gate insulator layer on the strain effect silicon layer. And the source drain which becomes the strain effect silicon layer in the both sid s of the gate electrode of a p-

chann l typ fi ld-effect transistor from p type diffusion layer is formed. Moreov r, it has the process of forming the source drain which becomes the strain effect silicon layer in the both sides of the gate electrode of an n channel type fi ld-eff ct transistor from n type diffusion layer.
[0016] By the manufacture method of the above-mentioned semiconductor device, since each source drain of a p-channel type and an n channel type field-effect transistor is formed only in the strain effect silicon layer, junction of each source drain is formed only in the strain effect silicon layer. Therefore, generating of junction leak with each source drain is suppressed. Moreover, since each source drain is formed in the one strain effect silicon layer and it is not necessary to manufacture the channel cambium corresponding to each source drain, a manufacture process becomes easy.
[0017] As for the semiconductor substrate which forms a logical circuit, the strain effect silicon layer is formed in the upper layer including the semiconductor device equipped with a p-channel type field-effect transistor in which the logical circuit gave [above-mentioned] explanation, and the n channel type field-effect transistor. Each source drain of a p-channel type and an n channel type field-effect transistor is formed only in the strain effect silicon layer.
[0018] In the above-mentioned logical circuit, since the source drain of each field-effect transistor is formed only in the strain effect silicon layer of the upper layer of a semiconductor substrate, junction of each source drain will exist in the strain effect silicon layer. Therefore, it is hard coming to generate junction leak.
[0019] A semiconductor substrate consists of a relaxed layer which consists of a silicon germanium layer which is what was formed on a germanium substrate and its germanium substrate, and by which stress is eased, and a strain effect silicon layer formed on the relaxed layer.
[0020] In the above-mentioned semiconductor substrate, since the germanium substrate is used, it is possible to form the relaxed layer which consists of a silicon germanium layer by which stress is eased directly, without forming a buffer layer on a germanium substrate. That is, since grid mismatching cannot occur easily between a germanium substrate and a relaxed layer, it becomes possible to adopt the above-mentioned composition. Therefore, the structure of a semiconductor substrate is simplified and the process which forms this semiconductor substrate is also simplified.
[0021]
[Embodiments of the Invention] The outline composition cross section of drawing 1 explains an example of the 1st operation gestalt concerning the field-effect transistor of this invention. Drawing 1 shows insulated-gate type n-MOSFET as an example.
[0022] p which changed germanium concentration in the thickness direction on the silicon substrate 21 as shown in drawing 1 - The buffer layer 22 which consists of silicon germanium (Si1-x Gex) of type, and p by which stress is eased - The relaxed layer 23 which consists of silicon germanium (Si1-x Gex) of type is formed in order.
[0023] The above-mentioned silicon substrate 21 is p which was able to be pulled up for example, by the CHOKURARU skiing (CZ) method. - It consists of type silicon. Moreover, the above-mentioned buffer layer 22 consists of silicon germanium which changed composition of germanium from x= 0.04 to x= 0.3 towards the upper layer side for example, from the silicon-substrate 21 side, for example, is formed in the thickness of about 1.6 micrometers. Moreover, composition of germanium consists of silicon germanium of x= 0.3, and the above-mentioned relaxed layer 23 is formed in the thickness of about 0.6 micrometers.
[0024] Furthermore on this relaxed layer 23, the strain effect silicon layer 24 used as the semiconductor layer which has the strain effect is formed as an example at the thickness of 13nm. as the thickness in which this strain effect silicon layer 24 can pull out the strain effect -- for example, the thickness of 5nm - about 30nm -- it is good if preferably formed in the thickness of 5nm - about 15nm Like the above, th semiconductor substrate 11 in which a field-effect transistor 1 is formed is constituted.
[0025] The field-effect transistor 1 explained below is formed in this semiconductor substrate 11. That is, on the above-mentioned strain effect silicon lay r 24, the gate electrode 13 is form d through the gate insulator layer 12, and the source drains 14 and 15 ar formed in the upper layer of the strain effect silicon layer 24 in the both sides of this gate electrode 13. The above-mentioned gate insulator layer 12 consists of a silicon oxide whose thickness is 6nm, and the above-mentioned gat electrode 13 consists of contest polysilicon. Moreover, as for the above-mentioned sourc drains 14 and 15, for

example, the junction depth is formed in about 5nm. Therefore, these source drains 14 and 15 will be formed only in the strain effect silicon layer 24 whose thickness is 13nm. The field-effect transistor 1 is constituted like the above.

[0026] The above-mentioned strain effect is explained here. The strain effect is the phenomenon in which the degree of electron transfer will become large if it says that the effective mass of a carrier changes when the energy band is distorted and tensile stress is received (the mobility of an electron hole becoming small), and the mobility of an electron hole will become large if compressive stress is received (the degree of electron transfer becomes small), when the thin film semiconductor receives stress in a thin film semiconductor.

[0027] in the above-mentioned field-effect transistor 1, since the source drains 14 and 15 (the junction depth is 5nm) are formed only in the strain effect silicon layer 24 whose thickness is 13nm, junction of the source drains 14 and 15 will exist in the strain effect silicon layer 24 Therefore, generating of junction leak of a field-effect transistor 1 is suppressed. Moreover, in a silicon network, the strain effect silicon layer 24 receives tensile stress by the difference of a lattice constant with the relaxed layer 23 which consists of silicon and silicon germanium of a ground. Since the channel layer of a field-effect transistor 1 will be formed in this strain effect silicon layer 24, degeneracy of the bottom of a conduction band is cleared, as for an electron, the effective mass becomes small, and mobility increases near the double precision. Therefore, the mutual conductance gm of a field-effect transistor 1 improves near the double precision as a nMOS transistor.

[0028] Next, the outline composition cross section of drawing 2 explains an example of the 2nd operation form concerning a field-effect transistor. In drawing 2 , the same sign is given to the same component part as aforementioned drawing 1 explained.

[0029] the field-effect transistor 1 which explained the field-effect transistor 2 by drawing 1 as shown in drawing 2 -- setting -- source drain 14 and 15 top -- being the so-called -- it accumulates and the source drains (or it is also called an EREBETEDDO source drain) 31 and 32 are formed It consists of these silicon epitaxial layers 33 and 34 with which it accumulates and is formed by the source drains 31 and 32 on the source drain 14 and 15, and refractory-metal silicide layers 35 and 36 currently formed in the silicon epitaxial layers 33 and 34. The above-mentioned silicon epitaxial layers 33 and 34 are formed in the thickness of about 50nm.

[0030] In addition, the offset insulator layer 16 is formed on the gate electrode 13, and the sidewall insulator layers 17 and 18 are formed in the side attachment wall of this gate electrode. By this, it accumulated with the gate electrode 13 and short-circuit with the source drains 31 and 32 is prevented. Moreover, the above-mentioned source drains 14 and 15 are good for the sidewall insulator layer 17 and the strain effect silicon layer 24 under 18 also as LDD (Lightly Doped Drain) structure in which the low concentration diffusion layer was formed. Moreover, the gate electrode 13 may be formed with polycide structure. With this polycide structure, the above-mentioned offset insulator layer 16 is not formed.

[0031] In the above-mentioned field-effect transistor 2, it becomes possible to reduce sheet resistance of the source drains 14 and 15, without silicide-izing the source drains 14 and 15 by having accumulated and having formed the source drains 31 and 32. Consequently, the high-speed operation of a field-effect transistor 2 becomes more possible to stability.

[0032] Next, the manufacturing process view of drawing 3 explains an example of the 1st operation form concerning the manufacture method of the field-effect transistor of this invention. In drawing 3 , the same sign is given to the same component part as aforementioned drawing 1 explained.

[0033] As shown in (1) of drawing 3 , with epitaxial growth technology, such as an ultra-high-vacuum chemical vapor-growth (UHV-CVD) method and molecular beam epitaxy [MBE (Molecular Beam Epitaxy)] p which changed germanium concentration in the thickness direction on the silicon substrate 21 - The buffer layer 22 which consists of silicon germanium (Si1-x Gex) of type For example, it forms in the thickness of 1.6 micrometers by changing composition of germanium to x= 0.3 from x= 0.04 towards an upper layer side, and depositing silicon germanium from a silicon-substrate 21 side. p which was able to be pulled up for example, by the CHOKURARU skiing [CZ (Czochralski)] method in the above-mentioned silicon substrate 21 - A type silicon substrate is used.

[0034] p by which stress is furth rmore eased on the above-mentioned buffer layer 22 - Composition of

germanium deposits the silicon germanium of x= 0.3 on the thickness of 0.6 micrometers, and forms the relaxed layer 23 which consists of silicon germanium of type. And the strain effect silicon layer 24 used as the semiconductor lay r which has the strain effect is formed as an xample on this relaxed layer 23 at the thickness of 13nm. the thickness in which this strain effect silicon layer 24 can pull out the strain effect, for example, the thickness of 5nm - 30nm, -- it is good if preferably formed in the thickness of 5nm - 15nm When UHV-CVD was adopted, for example as membrane formation conditions for the above-mentioned strain effect silicon layer 24, the mono silane [SiH4] (flow rate : 20sccm) or the disilane (Si two H6) (flow rate : 5sccm) was used for material gas, the pressure of membrane formation atmosphere was set as 1.33microPa, substrate temperature was set as about 600 degrees C, and film formation was performed. In addition, sccm expresses the volumetric flow rate (a part for cm3/) in reference condition.

[0035] In addition, it is desirable to form the above-mentioned buffer layer 22, the relaxed layer 23, and the strain effect silicon layer 24 continuously within the same chamber. In this case, by using a mono silane (SiH4), germane (GeH4), or a disilane (Si two H6) and germane (GeH4) for material gas, and changing each gas ratio suitably After forming the above-mentioned buffer layer 22 and the relaxed layer 23 by forming the silicon germanium layer of a desired component ratio, germane's supply is stopped and the strain effect silicon layer 24 is formed using a mono silane or a disilane.

[0036] In the strain effect silicon layer 24 formed by the above-mentioned method, tensile stress has arisen by the difference in the lattice constant of a silicon germanium layer (relaxed layer 23) and a silicon layer (the strain effect silicon layer 24). Thus, the semiconductor substrate 11 is formed.

[0037] Subsequently, as shown in (2) of drawing 3 , the gate insulator layer 12 is formed by the silicon oxide on the strain effect silicon layer 24. then, after depositing contest polysilicon and forming the gate electrode layer 41 (the portion shown according to a two-dot chain line is also included) by CVD, patterning of the resist film is carried out with formation of the resist film (illustration abbreviation) by resist application, and lithography technology, and the gate electrode 13 is formed by the gate electrode layer 41 with the formation which is a resist mask (illustration abbreviation), and the etching technology which used the resist mask for the etching mask By this etching, the portion shown according to the two-dot chain line of the gate insulator layer 12 also **********s.

[0038] as shown in (3) of drawing 3 after that, the ion implantation of the impurity for forming a source drain is carried out to the strain effect silicon layer 24 in the both sides of the gate electrode 13 with the ion-implantation which used the gate electrode 13 as the mask, and the source drains 14 and 15 which are n types are formed in the upper layer of the strain effect silicon layer 24

[0039] As the above-mentioned ion-implantation conditions, when arsenic ion (As+) is used for an impurity, the projection range of arsenic ion is set as 6nm for placing energy as 5keV(s), for example, and it is a dose 5x1015 pieces/cm 2 It set up. Then, activation annealing is performed. As this annealing condition, in the case of furnace annealing, for example, annealing temperature is set up as 800 degrees C, and annealing time is set up in 20 minutes. Moreover, when ELA (Excimer Laser Annealing) performs rapid heating annealing (RTA:Rapid Thermal Annealing), it is the energy of for example, an irradiation laser beam 1 J/cm2 It sets up. Moreover, by performing such activation annealing, the source drains 14 and 15 (the junction depth is about 6nm) of shallow junction are formed. In addition, in order to form shallow junction certainly, as for the above-mentioned annealing, it is desirable to carry out by RTA. Thus, a field-effect transistor 1 is formed.

[0040] In addition, although the above-mentioned source drains 14 and 15 were formed with the ion implantation, it is also possible to form, for example using methods, such as laser doping, gaseous-phase doping, and solid phase doping.

[0041] By the manufacture method of the above-mentioned field-effect transistor, since the source drains 14 and 15 of a field-effect transistor 1 are formed only in the strain effect silicon layer 24, junction of the source drains 14 and 15 will be formed only in the strain effect silicon layer 24. Therefore, as for the field-effect transistor 1 formed by this manufacture method, generating of junction leak was suppressed.

[0042] Next, the manufacturing process view of drawing 4 explains an example of the 2nd operation form concerning the manufacture method of a field-effect transistor. In drawing 4 , the sam sign is given to the same component part as aforementioned drawing 3 explain d.

[0043] In the manufacture method of a field-effect transistor explained by aforementioned drawing 3 , after forming the gate electrod layer 41 and forming the offset insulator layer 16 on the gate insulator lay r (41) used as the gate electrode 13 as shown in (1) of drawing 4 , patterning of th gat is performed. Subsequently, the sourc drains 14 and 15 are formed and the sidewall insulator layers 17 and 18 are formed after that. Then, alternatively, by the epitaxial grown method, silicon is alternatively deposited on the source drain 14 and 15, and the silicon epitaxial layers 33 and 34 are formed in the thickness of about 50nm. In addition, in making the above-mentioned source drains 14 and 15 into LDD (Lightly Doped Drain) structure, after performing patterning of the gate, it forms the low concentration diffusion layer which forms LDD structure in the strain effect silicon layer 24 of the lower part of the sidewall insulator layer formed behind with an ion implantation. Subsequently, after forming the sidewall insulator layers 17 and 18 in the side attachment wall of the gate electrode 13, the high concentration field of the above-mentioned source drains 14 and 15 is formed.

[0044] Subsequently, as shown in (2) of drawing 4 , the refractory-metal layer 37 is formed by sputtering or the chemical vapor-growth (CVD) method all over the silicon epitaxial layer 33 side and 34 sides. Then, heat-treat (for example, RTA), the silicon of the silicon epitaxial layers 33 and 34 and the metal of the refractory-metal layer 37 are made to react, and the refractory-metal silicide layers 35 and 36 are formed in the silicon epitaxial layers 33 and 34. The above-mentioned refractory-metal layer 37 is formed for example, in a titanium layer. In this case, the above-mentioned refractory-metal silicide layers 35 and 36 turn into a titanium silicide layer. Then, etching removes the unreacted refractory-metal layer 37 (portion shown according to a two-dot chain line) on the sidewall insulator layer 17 and 18 [the offset insulator layer 16 and], for example. Thus, on the source drain 14 and 15, it consists of refractory-metal silicide layers 35 and 36 formed in the silicon epitaxial layers 33 and 34, and accumulates, the source drains 31 and 32 are formed, and a field-effect transistor 2 is formed. In addition, in the above-mentioned silicide-izing, in forming the gate electrode 13 in polycide structure simultaneously, the above-mentioned offset insulator layer 16 forms the above-mentioned refractory-metal layer 37 in the state of contacting on the gate electrode 13 without forming.

[0045] By the manufacture method of the above-mentioned field-effect transistor 2, since it accumulates and the source drains 31 and 32 are formed by silicide-izing the upper part of the source drain 14 and the silicon epitaxial layers 33 and 34 deposited on 15, the source drains 14 and 15 are not silicide-ized. Therefore, where the source drains 14 and 15 of shallow junction are left, it becomes possible to reduce sheet resistance of the source drains 14 and 15.

[0046] Next, the outline composition cross section of drawing 5 explains an example of the 1st operation gestalt concerning the semiconductor device of this invention. In drawing 5 , the same sign is given to the same component part as aforementioned drawing 1 explained.

[0047] As shown in drawing 5 , the semiconductor substrate 11 is constituted as follows. That is, the buffer layer 22, the relaxed layer 23, and the strain effect silicon layer 24 are formed in order on the silicon substrate 21.

[0048] The above-mentioned silicon substrate 21 is p which was able to be pulled up for example, by the CHOKURARU skiing (CZ) method. - It consists of type silicon. Moreover, the above-mentioned buffer layer 22 is p which changed germanium concentration in the thickness direction. - It consists of silicon germanium which it consisted [germanium] of silicon germanium (Si1-x Gex) of type, for example, changed composition of germanium from x= 0.04 to x= 0.3 towards the upper layer side from the silicon-substrate 21 side, for example, is formed in the thickness of 1.6 micrometers.

[0049] Furthermore, the relaxed layer 23 is n by which stress is eased. - It consists of silicon germanium (Si0.7 germanium0.3) of type, and is formed in the thickness of 0.6 micrometers. Furthermore, the above-mentioned strain effect silicon layer 24 is formed in the thickness of 13nm as an example. This strain effect silicon layer 24 is the thickness which can pull out the strain effect. For example, what is necessary is to just be preferably formed in the thickness of 5nm - 15nm in 5nm - 30nm thickness.

[0050] Moreover, it is formed in the upper layer of the strain effect silicon layer 24 to the relaxed layer 23, applying the isolation field 51 of the trench structure of separating electrically the field in which the field-effect transistor 3 of the field in which the n channel type field-effect transistor 1 is formed, and a p-channel type is formed. the field applied to the upper layer of the strain effect silicon layer 24 in which

the field-effect transistor 1 of further an n channel type is formed, and the relaxed layer 23 -- p -- n wells 26 are formed in the field applied to the upper layer of the strain effect silicon layer 24 in which a well 25 is formed in and the p-channel type field-effect transistor 3 is formed, and the relaxed layer 23 Like the above, the semiconductor substrate 11 in which the semiconductor device 5 which consists of an n channel type field-effect transistor 1 and a p-channel type field-effect transistor 3 is formed is constituted.

[0051] The above-mentioned n channel type field-effect transistor 1 accomplishes the following composition. That is, in the upper layer of the strain effect silicon layer [in / the both sides of this gate electrode 13 / on the above-mentioned strain effect silicon layer 24, the gate electrode 13 is formed through the gate insulator layer 12, and] 24, it is n+. The source drains 14 and 15 which consist of a type diffusion layer are formed. The above-mentioned gate insulator layer 12 consists of a silicon oxide whose thickness is 13nm, and the above-mentioned gate electrode 13 consists of contest polysilicon. Moreover, as for the above-mentioned source drains 14 and 15, for example, the junction depth is formed in about 6nm. Therefore, these source drains 14 and 15 will be formed only in the strain effect silicon layer 24. The field-effect transistor 1 is constituted like the above.

[0052] On the other hand, the above-mentioned p-channel type field-effect transistor 3 accomplishes the following composition. That is, in the upper layer of the strain effect silicon layer [in / the both sides of this gate electrode 73 / on the above-mentioned strain effect silicon layer 24, the gate electrode 73 is formed through the gate insulator layer 72, and] 24, it is p+. The source drains 74 and 75 which consist of a type diffusion layer are formed. The above-mentioned gate insulator layer 72 consists of a silicon oxide whose thickness is 13nm, and the above-mentioned gate electrode 73 consists of contest polysilicon. Moreover, as for the above-mentioned source drains 74 and 75, for example, the junction depth is formed in about 7nm. Therefore, these source drains 74 and 75 will be formed only in the strain effect silicon layer 24. Like the above, the p-channel type field-effect transistor 3 is constituted.

[0053] In the above-mentioned semiconductor device 5, since the source drains 14 and 15 of the n channel type field-effect transistor 1 and the source drains 74 and 75 of the p-channel type field-effect transistor 3 are formed only in the strain effect silicon layer 24, each junction of the source drains 14 and 15 and the source drains 74 and 75 will exist in the strain effect silicon layer 24. Therefore, generating of junction leak stops being able to occur easily. Moreover, since the channel layer of the n channel type field-effect transistor 1 is formed in the strain effect silicon layer 24, a silicon network receives tensile stress by the difference of a lattice constant with the relaxed layer 23 which consists of silicon and silicon germanium of a ground. Therefore, degeneracy of the bottom of a conduction band is cleared, as for an electron, the effective mass becomes small, and the mobility within the inversion layer near the interface of silicon/silicon oxide increases near the double precision. Therefore, the mutual conductance gm as a nMOS transistor improves near the double precision. It becomes the conventional CMOS structure and almost equivalent structure from each source drains 14 and 15 and the source drains 74 and 75 being formed in the one more strain effect silicon layer 24. Therefore, structure becomes easy.

[0054] Although the above-mentioned semiconductor device 5 consists of one n channel type field-effect transistor 1 and one p-channel type field-effect transistor 3, it may consist of a two or more n channel type field-effect transistor 1 and a two or more p-channels type field-effect transistor 3.

[0055] Next, the outline composition cross section of drawing 6 explains an example of the 2nd operation form concerning a semiconductor device. In drawing 6 , the same sign is given to the same component part as aforementioned drawing 5 explained.

[0056] the field-effect transistor 1 which explained the field-effect transistor 2 by drawing 5 as shown in drawing 6 -- setting -- source drain 14 and 15 top -- being the so-called -- it accumulates and the source drains 31 and 32 are formed That is, it accumulates and the source drains 31 and 32 consist of the source drain 14, silicon epitaxial layers 33 and 34 currently formed on 15, and refractory-metal silicide layers 35 and 36 currently formed in the silicon epitaxial layers 33 and 34. In addition, the offs t insulator layer 16 is formed on the gate electrode 13, and the sidewall insulator lay rs 17 and 18 are formed in the side attachment wall of this gate electrode 13. Moreover, the above-mentioned source drains 14 and 15 are good for the sidewall insulator layer 17 and the strain effect silicon layer 24 under 18 also as LDD structure in which the low concentration diffusion lay r was formed.

[0057] the fi ld-effect transistor 3 which, on the other hand, xplain d th field-eff ct transistor 4 by drawing 5 -- setting – source drain 74 and 75 top -- being the so-called -- it accumulat s and the source drains 81 and 82 are formed That is, it accumulates and th source drains 81 and 82 consist of the source drain 74, silicon epitaxial layers 83 and 84 currently formed on 75, and refractory-metal silicide layers 85 and 86 currently formed in the silicon epitaxial layers 83 and 84. In addition, the offset insulator layer 76 is formed on the gate electrode 73, and the sidewall insulator layers 77 and 78 are formed in the side attachment wall of this gate electrode 73. Moreover, the above-mentioned source drains 74 and 75 are good for the sidewall insulator layer 77 and the strain effect silicon layer 24 under 78 also as LDD structure in which the low concentration diffusion layer was formed. Moreover, the gate electrodes 13 and 73 may be formed with polycide structure. With this polycide structure, the above-mentioned offset insulator layers 16 and 76 are not formed.
[0058] Without accumulating and silicide-izing the source drains 14 and 15 and the source drains 74 and 75 the source drains 31 and 32 and by having accumulated and having formed the source drains 81 and 82, the above-mentioned semiconductor device 5 enables it to reduce sheet resistance of the source drains 14 and 15 and the source drains 74 and 75, where shallow junction is maintained. Consequently, the high-speed operation of the wiring connected to the source drains 14 and 15 and the source drains 74 and 75 becomes possible.
[0059] The manufacturing process view of drawing 7 explains an example of the 1st operation form concerning the manufacture method of the semiconductor device of this invention. In drawing 7 , the same sign is given to the same component part as aforementioned drawing 5 explained.
[0060] By the same method as (1) of aforementioned drawing 3 explained, as shown in (1) of drawing 7 p which changed germanium concentration in the thickness direction on the silicon substrate 21 - The buffer layer 22 which consists of silicon germanium (Si1-x Gex) of type For example, it forms in the thickness of 1.6 micrometers by changing composition of germanium to x= 0.3 from x= 0.04 towards an upper layer side, and depositing silicon germanium from a silicon-substrate 21 side. p which was able to be pulled up by the CZ process in the above-mentioned silicon substrate 21 - A type silicon substrate is used.
[0061] n by which stress is furthermore eased on the above-mentioned buffer layer 22 - Composition of germanium deposits the silicon germanium of x= 0.3 on the thickness of about 0.6 micrometers, and forms the relaxed layer 23 which consists of silicon germanium of type. And the strain effect silicon layer 24 used as the semiconductor layer which has the strain effect is formed as an example on this relaxed layer 23 at the thickness of 13nm. the thickness in which this strain effect silicon layer 24 can pull out the strain effect, for example, the thickness of 5nm - 30nm, -- it is good if preferably formed in the thickness of 5nm - 15nm In this strain effect silicon layer 24, tensile stress has arisen by the difference in the lattice constant of a silicon germanium layer (relaxed layer 23) and a silicon layer (the strain effect silicon layer 24). Thus, the semiconductor substrate 11 is formed.
[0062] Then, it forms in the upper layer of the strain effect silicon layer 24 to the relaxed layer 23 by the formation method of the isolation field of the usual trench structure, applying the isolation field 51 of the trench structure of separating electrically the field in which the field-effect transistor 3 of the field in which the n channel type field-effect transistor 1 is formed, and a p-channel type is formed. In addition, the formation method of the isolation field of the above-mentioned usual trench structure is a method of forming the isolation field 51, by embedding an insulator layer in the trench and removing the excessive insulator layer on the semiconductor substrate 11 by etchback, chemical mechanical polishing, etc. after that, after forming a trench in the semiconductor substrate 11 with for example, lithography technology and etching technology.
[0063] subsequently, the field applied to the upper layer of the strain effect silicon layer 24 in which th n channel type field-effect transistor 1 is formed, and the relaxed layer 23 -- p -- a well 25 is formed with ion-implantation On n wells 26, for example, the resist mask (illustration ellipsis) is formed in that case. then, the field applied to the upper layer of the strain eff ct silicon layer 24 in which the p-chann l typ field-effect transistor 3 is formed, and the relaxed layer 23 aft r removing the abov -m ntioned resist mask -- n -- a w ll 26 is form d with ion-implantation On p w lls 25, for xampl , the resist mask (illustration ellipsis) is formed in that case. And this resist mask is removed after an ion implantation. In addition, whichever the n above-mentioned well 26 and p wells 25 form previously, inconvenience does

not have them. Her after, in (2) - (4) of drawing 7 , illustration of a part of silicon substrate 21 and buffer layer 22 is omitted.

[0064] Subsequently, by th same method, as shown in (2) of drawing 7 , the gate insulator layer 12 (72) is formed by th silicon oxide on the strain effect silicon layer 24 as (2) of aforementioned drawing 3 explained. Then, after depositing contest polysilicon and forming the gate electrode layer 41 (portion shown according to a two-dot chain line) by CVD, With the etching technology which carried out patterning of the resist film with formation of the resist film (illustration abbreviation) by resist application, and lithography technology, and used formation of a resist mask (illustration abbreviation), and its resist mask for the etching mask While forming the gate electrode 13 of an n channel type field-effect transistor which consists of a gate electrode layer 41 on the gate insulator layer 12, the gate electrode 73 of a p-channel type field-effect transistor which consists of a gate electrode layer 41 is formed on the gate insulator layer 72. By this etching, the portion shown according to the two-dot chain line of the gate insulator layer 12 (72) also **********s.

[0065] Subsequently, as shown in (3) of drawing 7 , after forming a wrap resist mask (illustration ellipsis) for the p well 25 top with a resist application and lithography technology, the ion implantation of the p type impurity for forming the source drain of a p-channel type field-effect transistor is carried out. in this ion implantation, the gate electrode 73 is used as a mask, the ion implantation for example, of the 2 boron-fluoride ion (BF2+) is carried out to the strain effect silicon layer 24 in the both sides of the gate electrode 73 as the above-mentioned p type impurity, and the source drains 74 and 75 of n mold are formed in the upper layer of the strain effect silicon layer 24 As the above-mentioned ion-implantation conditions, when 2 boron-fluoride ion (BF2+) is used for p type impurity, the projection range of 2 boron-fluoride ion is set as 5nm by setting placing energy to 5keV(s), and it is a dose 3x1015 pieces/cm, for example, 2 It set up. Then, for example, oxygen ashing and washing processing remove the above-mentioned resist mask. In addition, a thin oxide film (illustration ellipsis) may be formed before the ion implantation of the above-mentioned boron, and this thin oxide film may be removed after the ion implantation.

[0066] Then, as shown in (4) of drawing 7 , after forming a wrap resist mask (illustration abbreviation) for the n well 26 top with a resist application and lithography technology, the ion implantation of the n type impurity for forming the source drain of an n channel type field-effect transistor is carried out. in this ion implantation, the gate electrode 13 is used as a mask, the ion implantation of the arsenic ion (As+) is carried out to the strain effect silicon layer 24 in the both sides of the gate electrode 13 as the above-mentioned n type impurity, and the source drains 14 and 15 of n mold are formed in the upper layer of the strain effect silicon layer 24 As the above-mentioned ion-implantation conditions, when arsenic ion (As+) is used for n type impurity, the projection range of arsenic ion is set as 6nm for placing energy as 5keV(s), for example, and it is a dose 5x1015 pieces/cm 2 It set up.

[0067] Subsequently, for example, oxygen ashing and washing processing remove the above-mentioned resist mask. Then, activation annealing is performed. As this annealing condition, in the case of furnace annealing, for example, annealing temperature is set up as 800 degrees C, and annealing time is set up in 30 minutes. Moreover, in the case of rapid heating annealing [ELA (Excimer Laser Annealing)], it is the energy of an irradiation laser beam 1 J/cm2 It sets up. By performing such activation annealing, the source drains 14 and 15 of shallow junction are formed. Simultaneously, the source drains 74 and 75 are also activated by this activation annealing. Thus, the semiconductor device 5 which consists of an n channel field-effect transistor 1 and a p-channel field-effect transistor 3 is formed.

[0068] In addition, although the above-mentioned source drains 14 and 15 and the source drains 74 and 75 were formed with the ion implantation, it is also possible to form, for example using methods, such as laser doping, gaseous-phase doping, and solid phase doping.

[0069] By the manufacture method of the above-mentioned semiconductor device, since the source drains 14 and 15 of the n channel field-effect transistor 1 and the source drains 74 and 75 of the p-channel field-effect transistor 3 ar formed only in the strain effect silicon layer 24, each junction of the source drains 14 and 15 and the source drains 74 and 75 will be formed only in the strain effect silicon layer 24. Therefore, generating of junction leak is suppressed. Moreover, since each source drains 14 and 15 and the source drains 74 and 75 are formed in the one strain effect silicon layer 24 and it is not

n cessary to manufactur the channel cambium corresponding to each source drains 14 and 15 and the source drains 74 and 75, a manufacture process becomes easy.

[0070] Next, the manufacturing process view of drawing 8 explains an example of the 2nd operation form concerning the manufacture method of a semiconductor device below. In drawing 8 , the same sign is given to the same thing as the component part shown in aforementioned drawing 4 and drawing 6 .

[0071] In the manufacture method of the semiconductor device explained by aforementioned drawing 7 , after forming the gate electrode layer 41 and forming the offset insulator layer 16 on the gate insulator layer (41) used as the gate electrodes 13 and 73 as shown in (1) of drawing 8 , patterning of the gate is performed. Subsequently, the source drains 14 and 15 and the source drains 74 and 75 are formed, and the sidewall insulator layers 17 and 18 and the sidewall insulator layers 77 and 78 are formed after that. In addition, in making the above-mentioned source drains 14 and 15 and the source drains 74 and 75 into LDD (Lightly Doped Drain) structure, after performing patterning of the gate, it forms the low concentration diffusion layer which forms LDD structure with an ion implantation. In this case, LDD of a p-channel type field-effect transistor is formed by the p type low concentration diffusion layer, and LDD of an n channel type field-effect transistor is formed by the n type low concentration diffusion layer. Then, while forming the sidewall insulator layers 17 and 18 in the side attachment wall of the gate electrode 13, after forming the sidewall insulator layers 77 and 78 in the side attachment wall of the gate electrode 73, each high concentration field of the source drains 14 and 15 and the source drains 74 and 75 is formed with the impurity doping technology (for example, ion implantation) which is adapted for each.

[0072] Then, alternatively, by the epitaxial grown method, on the source drain 14 and 15, silicon is deposited alternatively and the silicon epitaxial layers 33 and 34 are formed. Simultaneously, on the source drain 74 and 75, silicon is deposited alternatively and the silicon epitaxial layers 83 and 84 are formed.

[0073] Subsequently, by the same method, as shown in (2) of drawing 8 , after forming the refractory-metal (for example, titanium) layer 37 all over the silicon epitaxial layer 33, 34, and 83 side and 84 sides, heat treatment (for example, RTA) is performed, the refractory-metal silicide (for example, titanium silicide) layers 35 and 36 are formed and accumulated on the silicon epitaxial layers 33 and 34, and the source drains 31 and 32 are formed as (2) of aforementioned drawing 4 explained. Simultaneously, the refractory-metal silicide (for example, titanium silicide) layers 85 and 86 are formed and accumulated on the silicon epitaxial layers 83 and 84, and the source drains 81 and 82 are formed. Then, etching removes the unreacted refractory-metal layer 37 (portion shown according to a two-dot chain line), for example. Thus, the semiconductor device 5 which consists of a field-effect transistor 2 which accumulated and formed the source drains 31 and 32, and a field-effect transistor 4 which accumulated and formed the source drains 81 and 82 is formed. In addition, in the above-mentioned silicide-izing, in forming the gate electrodes 13 and 73 in polycide structure simultaneously, the above-mentioned offset insulator layers 16 and 76 form the above-mentioned refractory-metal layer 37 in the gate electrode 13 and the state of contacting on 73 without forming.

[0074] By the manufacture method of the above-mentioned semiconductor device, since the upper part of the source drains 14, 15, and 74 and the silicon epitaxial layers 33, 34, 83, and 84 deposited on 75 is silicide-ized, and is accumulated and the source drains 31, 32, 81, and 82 are formed, the source drains 14, 15, 74, and 75 are not silicide-ized. For the reason, where shallow junction of the source drains 14 and 15 is maintained, it becomes possible to reduce sheet resistance of the source drains 14 and 15. Similarly, sheet resistance of the source drains 74 and 75 is also reduced.

[0075] Next, the circuit diagram of drawing 9 explains an example of the 1st operation form concerning the logical circuit of this invention. The following explanation attaches and explains the same sign to a thing like each component part explained by aforementioned drawing 1 and drawing 5 .

[0076] The logical circuit 111 shown in drawing 9 is ISSCC Dig.Tech.Papers and "Cascode Voltage Switch Logic:A Differential CMOS Logic Family". [Feb.] (1984) Heller, L.G.and Griffin, W.R., p16-17 It is equivalent to the circuitry currently indicated. And the n channel type field-effect transistors (nMOS) 112-115 which constitute logic, and the p-channel type field-effect transistor (pMOS) 121,122 which constitutes a pMOS intersection latch are formed in the strain effect silicon layer 24 formed in the upper

layer of the s miconductor substrate 11 explained by aforementioned drawing 1 and drawing 5 . This composition is the f ature of the logical circuit of this invention. That is, each source drain (illustration abbreviation) of the above 112-nMOS 115 is also formed only in the strain effect silicon layer 24, and each source drain (illustration abbreviation) of the above pMOS121,122 is formed only in th strain effect silicon layer 24.

[0077] In the above-mentioned logical circuit 111, since each source drain of nMOS 112-115 is formed only in the strain effect silicon layer 24, junction of each source drain will exist in the strain effect silicon layer 24. Therefore, since generating of junction leak stops being able to occur easily, improvement in the reliability of a logical circuit 111 can be aimed at. Moreover, in the above-mentioned logical circuit 111, logic consists of nMOS(s) 112-115, and the load is formed by the intersection latch of pMOS121,122. In this case, when an output changes and a pMOS intersection latch is reversed, while a direct current flows to a logical circuit and change of an output is completed, a direct current will not flow. Moreover, as a feature of this logical circuit 111, the electric field built over each transistor at the time of operation are eased. Therefore, since the fall of mobility does not take place, high-speed operation becomes possible. Moreover, since the channel layer of nMOS is formed in the strain effect silicon layer 24, a silicon network receives tensile stress by the difference of a lattice constant with the relaxed layer 23 which consists of silicon and silicon germanium of a ground. Therefore, degeneracy of the bottom of a conduction band is cleared, as for an electron, the effective mass becomes small, and mobility increases near the double precision. Therefore, the mutual conductance gm as a nMOS transistor improves near the double precision. On the other hand, since high performance is not demanded at pMOS121,122, the composition in a few element number is attained. Thus, the logical circuit in which high-speed operation is possible consists of low batteries.

[0078] Next, the circuit diagram of drawing 10 explains an example of the 2nd operation form concerning a logical circuit. The following explanation attaches and explains the same sign to a thing like each component part explained by aforementioned drawing 1 and drawing 5 .

[0079] The logical circuit 131 shown in drawing 10 is IEEE J.Solid-state Circuits, "A 3.8-ns CMOS 16x16-b Multiplier Using Complementary Pass-Transistor Logic, and "25. [2] (1990) Yano, K.et al., and p388-395 It is equivalent to the circuitry currently indicated and is one of the basic circuits using the pass transistor logic. That is, the logical circuit is constituted by the nMOS path transistor. And the n channel type field-effect transistors (nMOS) 132-135 which constitute a pass transistor logic, CMOS inverter 143,144, and the p-channel type field-effect transistor (pMOS) 141,142 which performs compensation of an output level are formed in the strain effect silicon layer 24 formed in the upper layer of the semiconductor substrate 11 explained by aforementioned drawing 1 and drawing 5 . This composition is the feature of the logical circuit of this invention. That is, each source drain (illustration abbreviation) of the above 132-nMOS 135 is also formed only in the strain effect silicon layer 24, and the source drain (illustration abbreviation) of the above pMOS141,142 and each source drain (illustration abbreviation) of CMOS inverter 143,144 are formed only in the strain effect silicon layer 24.

[0080] In the above-mentioned logical circuit 131, since each source drain of nMOS 112-115 is formed only in the strain effect silicon layer 24, junction of each source drain will exist in the strain effect silicon layer 24. Therefore, since generating of junction leak stops being able to occur easily, improvement in the reliability of a logical circuit 111 can be aimed at. Moreover, logic is constituted by the nMOS path transistor, and it has the driving force of a load reinforced in the above-mentioned logical circuit 131, for example while "H" level returns that only the threshold voltage of nMOS falls rather than VDD with CMOS inverter 143,144 formed in the output, when it lets the signal of "H" level pass for example, to a nMOS path transistor. Furthermore, an output level is compensated by the intersection latch of pMOS141,142. That is, "H" level is amended to VDD. Driving force is not needed for pMOS141,142 for that. In addition, what is necessary is to be large in the channel width of pMOS141,142, and just to design channel length small, in order to make it reversal operation of an intersection latch of pMOS141,142 not become slow.

[0081] Subsequently, the circuit diagram of drawing 11 explains an example of the 3rd operation form concerning a logical circuit. The following explanation attaches and explains the same sign to a thing like each component part explained by aforementioned drawing 1 and drawing 5 .

[0082] The logical circuit 151 shown in drawing 11 Proc.IEEE 1994 CICC and "A High Speed and

LowPower, Swing R stored Pass-Transistor Logic Based Multiply and Accumulate Circuit for Multimedia Applications and" [May.] (1994) Prameswer, A., Hara, H., and Sakurai, T., and p358-362 It is equivalent to th circuitry currently indicated and is one of the basic circuits using the pass transistor logic. That is, the nMOS pass transistor logic and the CMOS latch are used. And th n chann l type fi ld-effect transistors (nMOS) 152-155 which constitute a pass transistor logic, and the p-channel type field-effect transistor (pMOS) 161,162 which constitutes a CMOS latch and the n channel type field-effect transistor (nMOS) 163,164 are formed in the strain effect silicon layer 24 formed in the upper layer of the semiconductor substrate 11 explained by aforementioned drawing 1 and drawing 5 . This composition is the feature of the logical circuit of this invention. That is, each source drain (illustration abbreviation) of the above [nMOS / nMOS and / 163,164] 152-155 is also formed only in the strain effect silicon layer 24, and each source drain (illustration abbreviation) of the above pMOS161,162 is formed only in the strain effect silicon layer 24.

[0083] In the above-mentioned logical circuit 151, since each source drain of nMOS 112-115 is formed only in the strain effect silicon layer 24, junction of each source drain will exist in the strain effect silicon layer 24. Therefore, since generating of junction leak stops being able to occur easily, improvement in the reliability of a logical circuit 131 can be aimed at.

[0084] Furthermore, since a CMOS latch has the feature to which a margin of operation becomes large as compared with a pMOS intersection latch in order to operate with a push pull and static current does not flow, a working speed becomes quick. Therefore, rather than the aforementioned logical circuit 131, low-power-ization can be attained and high-speed operation becomes possible. Moreover, even if the ratio of each gate width of pMOS of the CMOS latch to the path transistor of nMOS composition and nMOS changes, it has the advantage which can take the large optimal field of a time delay. Therefore, the design margin has the advantage to which it becomes large and a manufacture margin also becomes large in connection with it.

[0085] In addition, the above-mentioned logical circuit 111,131,151 is an example, and it is possible to use the composition which forms a field-effect transistor 1 and a semiconductor device 5 for the strain effect silicon layer 24 explained to other logical circuits using the path transistor network, for example, DSL, (Differential Split-Level logic), DCVSPG (Differential Cascode Voltage Switch with the Pass-Gate), etc. by above-mentioned drawing 1 , drawing 5 , etc.

[0086] Next, the outline composition cross section of drawing 12 explains an example of the operation form concerning the semiconductor substrate of this invention. In drawing 12 , the same sign is given to the same thing as the component part explained by aforementioned drawing 1 .

[0087] As shown in drawing 12 , as for the semiconductor substrate 91, the strain effect silicon layer 24 which is a semiconductor layer in which the relaxed layer 23 is formed in and has the strain effect at a it top is formed on the germanium substrate 92. The above-mentioned relaxed layer 23 is n. - It consists of silicon germanium (Si0.7 germanium0.3) with which the stress of type (or p-) is eased, for example, is formed in the thickness of about 0.6 micrometers. In addition, the composition ratio of germanium is not limited to the above-mentioned value, and is chosen suitably. Moreover, the strain effect silicon layer 24 is the same as that of what was explained by aforementioned drawing 1 . The semiconductor substrate 91 is constituted like the above.

[0088] In the above-mentioned semiconductor substrate 91, since the germanium substrate 92 is used, it is possible to form the relaxed layer 23 which consists of a silicon germanium layer by which stress is eased directly, without forming a buffer layer on the germanium substrate 92. That is, since grid mismatching cannot occur easily between the germanium substrate 92 and the relaxed layer 23, it becomes possible to adopt the above-mentioned composition. Therefore, the structure of the semiconductor substrate 91 is simplified and the process which forms this semiconductor substrate 91 is also simplified.

[0089] Next, the above-mentioned semiconductor substrate 91 can form in the strain eff ct silicon layer 24 of the semiconductor substrate 91 the field-effect transistor 1 explained by aforementioned drawing 1 using the semiconductor substrate 91 explained by above-mentioned drawing 12 instead of the aforementioned semiconductor substrate 11 explained by aforementioned drawing 1 . Moreover, it is also possible to form in the strain effect silicon layer 24 of the semiconductor substrat 91 the semiconductor device 5 explained by aforementioned drawing 5 using the semiconductor substrate 91

explained by above-mentioned drawing 12 instead of the aforementioned semiconductor substrate 11 explained by aforementioned drawing 5 .

[0090]

[Effect of th Inv ntion] As mention d above, since the source drain is formed only in th strain effect silicon layer which is a semiconductor layer which has the strain effect according to the field-effect transistor of this invention as explained, junction of a source drain exists in the strain effect silicon layer. Therefore, since generating of junction leak stops being able to occur easily while being able to aim at improvement in the mobility of a transistor, it becomes possible to aim at improvement in a transistor p rformance.

[0091] Since the source drain of a field-effect transistor is formed only in the strain effect silicon layer which is a semiconductor layer which has the strain effect according to the manufacture method of the field-effect transistor of this invention, junction of a source drain can be formed only in the strain effect silicon layer. Therefore, generating of junction leak can be suppressed.

[0092] Since the source drain of a p-channel type field-effect transistor and the source drain of an n channel type field-effect transistor are formed only in the strain effect silicon layer which is a semiconductor layer which has the strain effect according to the semiconductor device of this invention, junction of each source drain exists in the strain effect silicon layer. Therefore, since generating of junction leak stops being able to occur easily while being able to aim at improvement in the mobility of a transistor, it becomes possible to aim at improvement in a transistor performance. Moreover, it becomes the conventional CMOS structure and almost equivalent structure from each source drain being formed in the one strain effect silicon layer. Therefore, structure becomes easy.

[0093] since the source drain of a p-channel field-effect transistor and the source drain of an n channel field-effect transistor are formed only in the strain effect silicon layer which is a semiconductor layer which has the strain effect according to the manufacture method of the semiconductor device of this invention, junction of each source drain accepts it in the strain effect silicon layer, is boiled, and can be formed Therefore, generating of junction leak can be suppressed. Moreover, since each source drain is formed in the one strain effect silicon layer and it is not necessary to manufacture the channel cambium corresponding to each source drain, simplification of a manufacture process can be attained.

[0094] Since according to the logical circuit of this invention the strain effect silicon layer is formed in the upper layer of a semiconductor substrate and the source drain of each field-effect transistor is formed only in the strain effect silicon layer, junction of each source drain exists in the strain effect silicon layer. Therefore, since generating of junction leak stops being able to occur easily while being able to aim at improvement in the mobility of a transistor, it becomes possible to aim at improvement in a transistor performance. Moreover, it becomes the conventional CMOS structure and almost equivalent structure from the source drain of each field-effect transistor being formed in the one strain effect silicon layer. Therefore, structure becomes easy.

[0095] According to the semiconductor substrate of this invention, since the germanium substrate is used, it becomes possible to form the relaxed layer which consists of a silicon germanium layer by which stress is eased directly, without forming a buffer layer on a germanium substrate. That is, since grid mismatching cannot occur easily between a germanium substrate and a relaxed layer, it becomes possible to adopt the above-mentioned composition. Therefore, the process which can simplify the structure of a semiconductor substrate and forms a semiconductor substrate can be simplified.

[Translation done.]

TECHNICAL FIELD

[The technical field to which invention belongs] this invention relates to the semiconductor substrate in which the logical circuit and th y which contain th field-effect transistor in_which the source drain was formed, the semiconductor devic containing the manufacture method and its field-effect transistor, and the manufacture method and its s miconductor d vice in the silicon lay r which has th strain effect in detail are formed about the logical circuit and the semiconductor substrate containing a fi ld-effect

transistor, the manufacture method and a semiconductor d vice, and the manufacture method and its semiconductor d vice.

[Translation done.]

PRIOR ART

[Description of the Prior Art] The device by the material using the strain (distortion) effect is becoming possible by progress of IV group semiconductor materials, such as silicon / silicon germanium, and a thin film coating technology, and the research which aimed at high efficiency and the low-battery device is very prosperous in it now. In a thin film semiconductor, an energy band is distorted and the above-mentioned strain effect means that the effective mass of a carrier changes, when a film receives str ss. it is becoming possible to form the semiconductor thin film which has this strain effect by devising multilayers, such as for example, silicon / silicon germanium, and controlling membranous internal stress by molecular beam epitaxy technology, chemical vapor-growth (UHV-CVD) technology under an ultra-high vacuum, etc. Thus, development of a highly efficient MOS system device, a sensor, etc. is also progressing by controlling a band-gap difference and a membranous strain by the heterojunction.
[0003] In the case of a silicon film, tensile stress will be received by the silicon film of the SOI (Silicon on insulator) substrate formed by the formation technology of a zone melt method and the single-crystal-silicon film by irradiation of an Ar ion laser etc. On the other hand, compressive stress will be received by the silicon film of an SOS (Silicon on Sapphire) substrate. Consequently, in the former, the degree of electron transfer becomes large, and the mobility of an electron hole becomes large in the latter. In other words, in the former, the mobility of an electron hole becomes small, and the degree of electron transfer becomes small by the latter.
[0004] Moreover, if depositing a silicon film on the epitaxial layer of the so-called silicon germanium in the relaxed state where stress is eased in the case of a silicon system MOS (Metal-Oxide-Semiconductor) transistor, speaking concretely, improvement in the degree of electron transfer can be aimed at with tensile stress (if it says strictly, the band which degenerated to six is explained to be divided into two bands with which effective masses differ). On the other hand, if the silicon germanium (so-called germanium rich silicon germanium) film containing many germanium is formed, improvement in the mobility of an electron hole can be aimed at with compressive stress.
[0005] Based on the property of such a strain effect silicon layer, the result of a high mutual conductance [gm (mobility)] is obtained by the MOS transistor which controlled and produced the stress of the layer which forms a multilayer and serves as a channel. Appl.Phys.Letter (USA), 63 (1993) S.P.Voinigensen et al., and p660 And IEEE Electronic Devices (USA), 43 (1996) L.H.Jiang and R.G.Elliman, and p97 **** – the pMOS transistor is indicated Moreover, Appl.Phys.Letter (USA), 64 (1994) KIsmail et al., and p3124 (1994) And the nMOS transistor is indicated by IEDM 94-37 (USA) and J.Welser et al.
[0006] On the other hand, the path transistor is proposed as latest highly efficient logic (LOGIC) which performs low-battery operation, and the proposal in the latest applied-technology fields, such as CPU (Central Processig Unit) and MPEG (Moving Picture Experts Group), is made. Such a logical circuit requires the highly efficient property that the nMOS transistor used as a subject has a high mutual conductance in low-battery operation. On the other hand, even if there are few element numbers at precharge usage [a pMOS transistor] etc., a demand is not carried out but the working speed like a nMOS transistor determines a performance by adjustment of channel width W, it is not disadvantageous in area.

[Translation done.]

EFFECT OF THE INVENTION

[Effect of the Invention] As mentioned above, since the source drain is formed only in the strain effect silicon layer which is a semiconductor layer which has the strain effect according to the field-effect transistor of this invention as explained, junction of a source drain exists in the strain effect silicon layer. Therefore, since generating of junction leak stops being able to occur easily while being able to aim at improvement in the mobility of a transistor, it becomes possible to aim at improvement in a transistor p rformance.

[0091] Since the source drain of a field-effect transistor is formed only in the strain effect silicon layer which is a semiconductor layer which has the strain effect according to the manufacture method of the fi ld-effect transistor of this invention, junction of a source drain can be formed only in the strain effect silicon layer. Therefore, generating of junction leak can be suppressed.

[0092] Since the source drain of a p-channel type field-effect transistor and the source drain of an n channel type field-effect transistor are formed only in the strain effect silicon layer which is a s miconductor layer which has the strain effect according to the semiconductor device of this invention, junction of each source drain exists in the strain effect silicon layer. Therefore, since generating of junction leak stops being able to occur easily while being able to aim at improvement in the mobility of a transistor, it becomes possible to aim at improvement in a transistor performance. Moreover, it becomes the conventional CMOS structure and almost equivalent structure from each source drain being formed in the one strain effect silicon layer. Therefore, structure becomes easy.

[0093] since the source drain of a p-channel field-effect transistor and the source drain of an n channel field-effect transistor are formed only in the strain effect silicon layer which is a semiconductor layer which has the strain effect according to the manufacture method of the semiconductor device of this invention, junction of each source drain accepts it in the strain effect silicon layer, is boiled, and can be formed Therefore, generating of junction leak can be suppressed. Moreover, since each source drain is formed in the one strain effect silicon layer and it is not necessary to manufacture the channel cambium corresponding to each source drain, simplification of a manufacture process can be attained.

[0094] Since according to the logical circuit of this invention the strain effect silicon layer is formed in the upper layer of a semiconductor substrate and the source drain of each field-effect transistor is formed only in the strain effect silicon layer, junction of each source drain exists in the strain effect silicon layer. Therefore, since generating of junction leak stops being able to occur easily while being able to aim at improvement in the mobility of a transistor, it becomes possible to aim at improvement in a transistor performance. Moreover, it becomes the conventional CMOS structure and almost equivalent structure from the source drain of each field-effect transistor being formed in the one strain effect silicon layer. Therefore, structure becomes easy.

[0095] According to the semiconductor substrate of this invention, since the germanium substrate is used, it becomes possible to form the relaxed layer which consists of a silicon germanium layer by which stress is eased directly, without forming a buffer layer on a germanium substrate. That is, since grid mismatching cannot occur easily between a germanium substrate and a relaxed layer, it becomes possible to adopt the above-mentioned composition. Therefore, the process which can simplify the structure of a semiconductor substrate and forms a semiconductor substrate can be simplified.

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] however, with the pMOS transistor and nMOS transistor in a Prior art which gave [above-m ntioned] explanation, since junction of a source drain is located in the small silicon germanium layer of a band gap when application by the highly effici nt low battery is considered, and since junction of a source drain is formed in silicon / silicon germanium interface, the existence which is leak serves as a technical problem

[Translation done.]

MEANS

[Means for Solving the Problem] this invention is a semiconductor substrate at the logical circuit row containing the field-effect transistor made in order to solve the above-mentioned technical problem and its manufacture method, a semiconductor device and its manufacture method, and its semiconductor d vice.

[0009] a field-effect transistor is formed in the silicon layer (henceforth the strain effect silicon layer) which is a semiconductor layer which has the strain effect currently formed in the semiconductor substrate upper layer, and the source drain of this field-effect transistor is formed in the strain effect silicon layer chisel

[0010] In the above-mentioned field-effect transistor, since the source drain is formed only in the strain effect silicon layer, junction of a source drain will exist in the strain effect silicon layer. Therefore, generating of junction leak stops being able to occur easily.

[0011] The manufacture method of a field-effect transistor forms the silicon layer (the strain effect silicon layer) which is a semiconductor layer which has the strain effect it is ineffective in the upper layer of a semiconductor substrate, and constitutes this semiconductor substrate. Then, a gate electrode is formed through a gate insulator layer on the strain effect silicon layer. And it is the manufacture method equipped with the process of forming a source drain, by doping the impurity for forming a source drain in the silicon layer which has the strain effect in the both sides of a gate electrode.

[0012] By the manufacture method of the above-mentioned field-effect transistor, since the source drain of a field-effect transistor is formed only in the strain effect silicon layer, junction of a source drain will be formed only in the strain effect silicon layer. Therefore, generating of junction leak is suppressed.

[0013] the p-channel type field-effect transistor and n channel type field-effect transistor which were formed in the silicon layer (the strain effect silicon layer) which is a semiconductor layer which has the strain effect currently formed on the semiconductor substrate including a field-effect transistor in which the semiconductor device gave [above-mentioned] explanation -- since -- it becomes and each source drain of a p-channel type and an n channel type field-effect transistor is formed only in the strain effect silicon layer

[0014] In the above-mentioned semiconductor device, since each source drain of a p-channel type and an n channel type field-effect transistor is formed only in the strain effect silicon layer, junction of each source drain will exist in the strain effect silicon layer. Therefore, it is hard coming to generate junction leak. Moreover, it becomes the conventional CMOS structure and almost equivalent structure from each source drain being formed in the one strain effect silicon layer. Therefore, structure becomes easy.

[0015] The manufacture method of a semiconductor device forms the strain effect silicon layer used as the upper layer of a semiconductor substrate, and constitutes this semiconductor substrate. The gate electrode of a p-channel type field-effect transistor and the gate electrode of an n channel type field-effect transistor are formed through a gate insulator layer on the strain effect silicon layer. And the source drain which becomes the strain effect silicon layer in the both sides of the gate electrode of a p-channel type field-effect transistor from p type diffusion layer is formed. Moreover, it has the process of forming the source drain which becomes the strain effect silicon layer in the both sides of the gate electrode of an n channel type field-effect transistor from n type diffusion layer.

[0016] By the manufacture method of the above-mentioned semiconductor device, since each source drain of a p-channel type and an n channel type field-effect transistor is formed only in the strain effect silicon layer, junction of each source drain is formed only in the strain effect silicon layer. Therefore, generating of junction leak with each source drain is suppressed. Moreover, since each source drain is formed in the one strain effect silicon layer and it is not necessary to manufacture the channel cambium

corresponding to each source drain, a manufacture process becomes easy.
[0017] As for the semiconductor substrate which forms a logical circuit, the strain effect silicon layer is formed in the upper layer including the semiconductor device equipp d with a p-channel type field-effect transistor in which th logical circuit gave [above-mentioned] explanation, and the n channel type field-effect transistor. Each source drain of a p-channel type and an n channel type field-effect transistor is formed only in the strain effect silicon layer.
[0018] In the above-mentioned logical circuit, since the source drain of each field-effect transistor is formed only in the strain effect silicon layer of the upper layer of a semiconductor substrate, junction of each source drain will exist in the strain effect silicon layer. Therefore, it is hard coming to generate junction leak.
[0019] A semiconductor substrate consists of a relaxed layer which consists of a silicon germanium layer which is what was formed on a germanium substrate and its germanium substrate, and by which stress is eased, and a strain effect silicon layer formed on the relaxed layer.
[0020] In the above-mentioned semiconductor substrate, since the germanium substrate is used, it is possible to form the relaxed layer which consists of a silicon germanium layer by which stress is eased directly, without forming a buffer layer on a germanium substrate. That is, since grid mismatching cannot occur easily between a germanium substrate and a relaxed layer, it becomes possible to adopt the above-mentioned composition. Therefore, the structure of a semiconductor substrate is simplified and the process which forms this semiconductor substrate is also simplified.
[0021]
[Embodiments of the Invention] The outline composition cross section of drawing 1 explains an example of the 1st operation gestalt concerning the field-effect transistor of this invention. Drawing 1 shows insulated-gate type n-MOSFET as an example.
[0022] p which changed germanium concentration in the thickness direction on the silicon substrate 21 as shown in drawing 1 - The buffer layer 22 which consists of silicon germanium (Si1-x Gex) of type, and p by which stress is eased - The relaxed layer 23 which consists of silicon germanium (Si1-x Gex) of type is formed in order.
[0023] The above-mentioned silicon substrate 21 is p which was able to be pulled up for example, by the CHOKURARU skiing (CZ) method. - It consists of type silicon. Moreover, the above-mentioned buffer layer 22 consists of silicon germanium which changed composition of germanium from x= 0.04 to x= 0.3 towards the upper layer side for example, from the silicon-substrate 21 side, for example, is formed in the thickness of about 1.6 micrometers. Moreover, composition of germanium consists of silicon germanium of x= 0.3, and the above-mentioned relaxed layer 23 is formed in the thickness of about 0.6 micrometers.
[0024] Furthermore on this relaxed layer 23, the strain effect silicon layer 24 used as the semiconductor layer which has the strain effect is formed as an example at the thickness of 13nm. as the thickness in which this strain effect silicon layer 24 can pull out the strain effect -- for example, the thickness of 5nm - about 30nm -- it is good if preferably formed in the thickness of 5nm - about 15nm Like the above, the semiconductor substrate 11 in which a field-effect transistor 1 is formed is constituted.
[0025] The field-effect transistor 1 explained below is formed in this semiconductor substrate 11. That is, on the above-mentioned strain effect silicon layer 24, the gate electrode 13 is formed through the gate insulator layer 12, and the source drains 14 and 15 are formed in the upper layer of the strain effect silicon layer 24 in the both sides of this gate electrode 13. The above-mentioned gate insulator layer 12 consists of a silicon oxide whose thickness is 6nm, and the above-mentioned gate electrode 13 consists of contest polysilicon. Moreover, as for the above-mentioned source drains 14 and 15, for example, the junction depth is formed in about 5nm. Therefore, these source drains 14 and 15 will be formed only in the strain effect silicon layer 24 whose thickness is 13nm. The field-effect transistor 1 is constituted like the above.
[0026] The above-mentioned strain effect is explained here. The strain effect is the phenomenon in which the degree of electron transfer will become large if it says that the effective mass of a carrier changes when the energy band is distorted and tensile stress is received (the mobility of an electron hole becoming small), and the mobility of an electron hole will becom large if compressiv stress is received (the degree of electron transfer becomes small), when the thin film semiconductor receives

stress in a thin film semiconductor.
[0027] in the above-mentioned field-effect transistor 1, since the source drains 14 and 15 (the junction depth is 5nm) are formed only in the strain effect silicon layer 24 whose thickness is 13nm, junction of the source drains 14 and 15 will exist in the strain effect silicon layer 24 Therefore, generating of junction leak of a field-effect transistor 1 is suppressed. Moreover, in a silicon network, the strain effect silicon layer 24 receives tensile stress by the difference of a lattice constant with the relaxed layer 23 which consists of silicon and silicon germanium of a ground. Since the channel layer of a field-effect transistor 1 will be formed in this strain effect silicon layer 24, degeneracy of the bottom of a conduction band is cleared, as for an electron, the effective mass becomes small, and mobility increases near the double precision. Therefore, the mutual conductance gm of a field-effect transistor 1 improves near the double precision as a nMOS transistor.
[0028] Next, the outline composition cross section of drawing 2 explains an example of the 2nd operation gestalt concerning a field-effect transistor. In drawing 2 , the same sign is given to the same component part as aforementioned drawing 1 explained.
[0029] the field-effect transistor 1 which explained the field-effect transistor 2 by drawing 1 as shown in drawing 2 -- setting -- source drain 14 and 15 top -- being the so-called -- it accumulates and the source drains (or it is also called an EREBETEDDO source drain) 31 and 32 are formed It consists of these silicon epitaxial layers 33 and 34 with which it accumulates and is formed by the source drains 31 and 32 on the source drain 14 and 15, and refractory-metal silicide layers 35 and 36 currently formed in the silicon epitaxial layers 33 and 34. The above-mentioned silicon epitaxial layers 33 and 34 are formed in the thickness of about 50nm.
[0030] In addition, the offset insulator layer 16 is formed on the gate electrode 13, and the sidewall insulator layers 17 and 18 are formed in the side attachment wall of this gate electrode. By this, it accumulated with the gate electrode 13 and short-circuit with the source drains 31 and 32 is prevented. Moreover, the above-mentioned source drains 14 and 15 are good for the sidewall insulator layer 17 and the strain effect silicon layer 24 under 18 also as LDD (Lightly Doped Drain) structure in which the low concentration diffusion layer was formed. Moreover, the gate electrode 13 may be formed with polycide structure. With this polycide structure, the above-mentioned offset insulator layer 16 is not formed.
[0031] In the above-mentioned field-effect transistor 2, it becomes possible to reduce sheet resistance of the source drains 14 and 15, without silicide-izing the source drains 14 and 15 by having accumulated and having formed the source drains 31 and 32. Consequently, the high-speed operation of a field-effect transistor 2 becomes more possible to stability.
[0032] Next, the manufacturing process view of drawing 3 explains an example of the 1st operation gestalt concerning the manufacture method of the field-effect transistor of this invention. In drawing 3 , the same sign is given to the same component part as aforementioned drawing 1 explained.
[0033] As shown in (1) of drawing 3 , with epitaxial growth technology, such as an ultra-high-vacuum chemical vapor-growth (UHV-CVD) method and molecular beam epitaxy [MBE (Molecular Beam Epitaxy)] p which changed germanium concentration in the thickness direction on the silicon substrate 21 - The buffer layer 22 which consists of silicon germanium (Si1-x Gex) of type For example, it forms in the thickness of 1.6 micrometers by changing composition of germanium to x= 0.3 from x= 0.04 towards an upper layer side, and depositing silicon germanium from a silicon-substrate 21 side. p which was able to be pulled up for example, by the CHOKURARU skiing [CZ (Czochralski)] method in the above-mentioned silicon substrate 21 - A type silicon substrate is used.
[0034] p by which stress is furthermore eased on the above-mentioned buffer layer 22 - Composition of germanium deposits the silicon germanium of x= 0.3 on the thickness of 0.6 micrometers, and forms the relaxed layer 23 which consists of silicon germanium of type. And the strain effect silicon layer 24 used as the semiconductor layer which has the strain effect is formed as an example on this relaxed layer 23 at the thickness of 13nm. the thickness in which this strain effect silicon layer 24 can pull out the strain effect, for example, the thickn ss of 5nm - 30nm, -- it is good if preferably formed in the thickness of 5nm - 15nm When UHV-CVD was adopted, for example as membrane formation conditions for the above-mentioned strain ffect silicon layer 24, the mono silane [SiH4] (flow rate : 20sccm) or the disilane (Si two H6) (flow rate : 5sccm) was us d for mat rial gas, the pressure of

membrane formation atmosphere was set as 1.33microPa, substrate temperature was set as about 600 degrees C, and film formation was performed. In addition, sccm expresses the volum tric flow rate (a part for cm3/) in reference condition.

[0035] In addition, it is desirabl to form the above-mentioned buffer layer 22, the relaxed layer 23, and the strain effect silicon layer 24 continuously within the same chamber. In this case, by using a mono silane (SiH4), germane (GeH4), or a disilane (Si two H6) and germane (GeH4) for material gas, and changing each gas ratio suitably After forming the above-mentioned buffer layer 22 and the relaxed layer 23 by forming the silicon germanium layer of a desired component ratio, germane's supply is stopped and the strain effect silicon layer 24 is formed using a mono silane or a disilane.

[0036] In the strain effect silicon layer 24 formed by the above-mentioned method, tensile stress has arisen by the difference in the lattice constant of a silicon germanium layer (relaxed layer 23) and a silicon layer (the strain effect silicon layer 24). Thus, the semiconductor substrate 11 is formed.

[0037] Subsequently, as shown in (2) of drawing 3 , the gate insulator layer 12 is formed by the silicon oxide on the strain effect silicon layer 24. then, after depositing contest polysilicon and forming the gate electrode layer 41 (the portion shown according to a two-dot chain line is also included) by CVD, patterning of the resist film is carried out with formation of the resist film (illustration abbreviation) by resist application, and lithography technology, and the gate electrode 13 is formed by the gate electrode layer 41 with the formation which is a resist mask (illustration abbreviation), and the etching technology which used the resist mask for the etching mask By this etching, the portion shown according to the two-dot chain line of the gate insulator layer 12 also **********s.

[0038] as shown in (3) of drawing 3 after that, the ion implantation of the impurity for forming a source drain is carried out to the strain effect silicon layer 24 in the both sides of the gate electrode 13 with the ion-implantation which used the gate electrode 13 as the mask, and the source drains 14 and 15 which are n types are formed in the upper layer of the strain effect silicon layer 24

[0039] As the above-mentioned ion-implantation conditions, when arsenic ion (As+) is used for an impurity, the projection range of arsenic ion is set as 6nm for placing energy as 5keV(s), for example, and it is a dose 5x1015 pieces/cm 2 It set up. Then, activation annealing is performed. As this annealing condition, in the case of furnace annealing, for example, annealing temperature is set up as 800 degrees C, and annealing time is set up in 20 minutes. Moreover, when ELA (Excimer Laser Annealing) performs rapid heating annealing (RTA:Rapid Thermal Annealing), it is the energy of for example, an irradiation laser beam 1 J/cm2 It sets up. Moreover, by performing such activation annealing, the source drains 14 and 15 (the junction depth is about 6nm) of shallow junction are formed. In addition, in order to form shallow junction certainly, as for the above-mentioned annealing, it is desirable to carry out by RTA. Thus, a field-effect transistor 1 is formed.

[0040] In addition, although the above-mentioned source drains 14 and 15 were formed with the ion implantation, it is also possible to form, for example using methods, such as laser doping, gaseous-phase doping, and solid phase doping.

[0041] By the manufacture method of the above-mentioned field-effect transistor, since the source drains 14 and 15 of a field-effect transistor 1 are formed only in the strain effect silicon layer 24, junction of the source drains 14 and 15 will be formed only in the strain effect silicon layer 24. Therefore, as for the field-effect transistor 1 formed by this manufacture method, generating of junction leak was suppressed.

[0042] Next, the manufacturing process view of drawing 4 explains an example of the 2nd operation form concerning the manufacture method of a field-effect transistor. In drawing 4 , the same sign is given to the same component part as aforementioned drawing 3 explained.

[0043] In the manufacture method of a field-effect transistor explained by aforementioned drawing 3 , after forming the gate electrode layer 41 and forming the offset insulator layer 16 on the gate insulator layer (41) used as the gate electrode 13 as shown in (1) of drawing 4 , patterning of the gate is performed. Subsequently, the source drains 14 and 15 are formed and th sidewall insulator lay rs 17 and 18 are formed after that. Then, alternatively, by the epitaxial grown method, silicon is alternatively deposited on the source drain 14 and 15, and the silicon epitaxial lay rs 33 and 34 are formed in the thickness of about 50nm. In addition, in making the above-mentioned sourc drains 14 and 15 into LDD (Lightly Doped Drain) structur , after performing patterning of the gat , it forms the low conc ntration

diffusion layer which forms LDD structure in the strain effect silicon layer 24 of the lower part of the sidewall insulator layer formed behind with an ion implantation. Subsequently, after forming the sidewall insulator layers 17 and 18 in the side attachment wall of the gate electrode 13, the high concentration fi ld of the above-m ntioned source drains 14 and 15 is formed.

[0044] Subsequently, as shown in (2) of drawing 4 , the refractory-metal layer 37 is formed by sputtering or the chemical vapor-growth (CVD) method all over the silicon epitaxial layer 33 side and 34 sides. Then, heat-treat (for example, RTA), the silicon of the silicon epitaxial layers 33 and 34 and the metal of the refractory-metal layer 37 are made to react, and the refractory-metal silicide layers 35 and 36 are formed in the silicon epitaxial layers 33 and 34. The above-mentioned refractory-metal layer 37 is formed for example, in a titanium layer. In this case, the above-mentioned refractory-metal silicide layers 35 and 36 turn into a titanium silicide layer. Then, etching removes the unreacted refractory-metal layer 37 (portion shown according to a two-dot chain line) on the sidewall insulator layer 17 and 18 [the offset insulator layer 16 and], for example. Thus, on the source drain 14 and 15, it consists of refractory-metal silicide layers 35 and 36 formed in the silicon epitaxial layers 33 and 34, and accumulates, the source drains 31 and 32 are formed, and a field-effect transistor 2 is formed. In addition, in the above-mentioned silicide-izing, in forming the gate electrode 13 in polycide structure simultaneously, the above-mentioned offset insulator layer 16 forms the above-mentioned refractory-metal layer 37 in the state of contacting on the gate electrode 13 without forming.

[0045] By the manufacture method of the above-mentioned field-effect transistor 2, since it accumulates and the source drains 31 and 32 are formed by silicide-izing the upper part of the source drain 14 and the silicon epitaxial layers 33 and 34 deposited on 15, the source drains 14 and 15 are not silicide-ized. Therefore, where the source drains 14 and 15 of shallow junction are left, it becomes possible to reduce sheet resistance of the source drains 14 and 15.

[0046] Next, the outline composition cross section of drawing 5 explains an example of the 1st operation form concerning the semiconductor device of this invention. In drawing 5 , the same sign is given to the same component part as aforementioned drawing 1 explained.

[0047] As shown in drawing 5 , the semiconductor substrate 11 is constituted as follows. That is, the buffer layer 22, the relaxed layer 23, and the strain effect silicon layer 24 are formed in order on the silicon substrate 21.

[0048] The above-mentioned silicon substrate 21 is p which was able to be pulled up for example, by the CHOKURARU skiing (CZ) method. - It consists of type silicon. Moreover, the above-mentioned buffer layer 22 is p which changed germanium concentration in the thickness direction. - It consists of silicon germanium which it consisted [germanium] of silicon germanium (Si1-x Gex) of type, for xample, changed composition of germanium from x= 0.04 to x= 0.3 towards the upper layer side from the silicon-substrate 21 side, for example, is formed in the thickness of 1.6 micrometers.

[0049] Furthermore, the relaxed layer 23 is n by which stress is eased. - It consists of silicon germanium (Si0.7 germanium0.3) of type, and is formed in the thickness of 0.6 micrometers. Furthermore, the above-mentioned strain effect silicon layer 24 is formed in the thickness of 13nm as an example. This strain effect silicon layer 24 is the thickness which can pull out the strain effect. For example, what is necessary is to just be preferably formed in the thickness of 5nm - 15nm in 5nm - 30nm thickness.

[0050] Moreover, it is formed in the upper layer of the strain effect silicon layer 24 to the relaxed layer 23, applying the isolation field 51 of the trench structure of separating electrically the field in which the field-effect transistor 3 of the field in which the n channel type field-effect transistor 1 is formed, and a p-channel type is formed. the field applied to the upper layer of the strain effect silicon layer 24 in which the field-effect transistor 1 of further an n channel type is formed, and the relaxed layer 23 -- p -- n wells 26 are formed in the field applied to the upper layer of the strain effect silicon layer 24 in which a well 25 is formed in and the p-channel type field-effect transistor 3 is formed, and th relaxed layer 23 Like the above, the semiconductor substrate 11 in which the semiconductor device 5 which consists of an n channel type field-effect transistor 1 and a p-channel type field-effect transistor 3 is form d is constituted.

[0051] The above-mentioned n channel type field-effect transistor 1 accomplishes the following composition. That is, in the upper layer of the strain effect silicon layer [in / the both sides of this gate

electrode 13 / on the above-mentioned strain effect silicon layer 24, the gate electrode 13 is formed through the gate insulator layer 12, and] 24, it is n+. The source drains 14 and 15 which consist of a type diffusion lay r are formed. Th above-mentioned gate insulator layer 12 consists of a silicon oxide whose thickness is 13nm, and the abov -mentioned gate electrod 13 consists of cont st polysilicon. Moreover, as for the above-mentioned source drains 14 and 15, for example, the junction depth is formed in about 6nm. Therefore, these source drains 14 and 15 will be formed only in the strain effect silicon layer 24. The field-effect transistor 1 is constituted like the above.

[0052] On the other hand, the above-mentioned p-channel type field-effect transistor 3 accomplishes the following composition. That is, in the upper layer of the strain effect silicon layer [in / the both sides of this gate electrode 73 / on the above-mentioned strain effect silicon layer 24, the gate electrode 73 is formed through the gate insulator layer 72, and] 24, it is p+. The source drains 74 and 75 which consist of a type diffusion layer are formed. The above-mentioned gate insulator layer 72 consists of a silicon oxide whose thickness is 13nm, and the above-mentioned gate electrode 73 consists of contest polysilicon. Moreover, as for the above-mentioned source drains 74 and 75, for example, the junction depth is formed in about 7nm. Therefore, these source drains 74 and 75 will be formed only in the strain effect silicon layer 24. Like the above, the p-channel type field-effect transistor 3 is constituted.

[0053] In the above-mentioned semiconductor device 5, since the source drains 14 and 15 of the n channel type field-effect transistor 1 and the source drains 74 and 75 of the p-channel type field-effect transistor 3 are formed only in the strain effect silicon layer 24, each junction of the source drains 14 and 15 and the source drains 74 and 75 will exist in the strain effect silicon layer 24. Therefore, generating of junction leak stops being able to occur easily. Moreover, since the channel layer of the n channel type field-effect transistor 1 is formed in the strain effect silicon layer 24, a silicon network receives tensile stress by the difference of a lattice constant with the relaxed layer 23 which consists of silicon and silicon germanium of a ground. Therefore, degeneracy of the bottom of a conduction band is cleared, as for an electron, the effective mass becomes small, and the mobility within the inversion layer near the interface of silicon/silicon oxide increases near the double precision. Therefore, the mutual conductance gm as a nMOS transistor improves near the double precision. It becomes the conventional CMOS structure and almost equivalent structure from each source drains 14 and 15 and the source drains 74 and 75 being formed in the one more strain effect silicon layer 24. Therefore, structure becomes easy.

[0054] Although the above-mentioned semiconductor device 5 consists of one n channel type field-effect transistor 1 and one p-channel type field-effect transistor 3, it may consist of a two or more n channel type field-effect transistor 1 and a two or more p-channels type field-effect transistor 3.

[0055] Next, the outline composition cross section of drawing 6 explains an example of the 2nd operation form concerning a semiconductor device. In drawing 6 , the same sign is given to the same component part as aforementioned drawing 5 explained.

[0056] the field-effect transistor 1 which explained the field-effect transistor 2 by drawing 5 as shown in drawing 6 -- setting -- source drain 14 and 15 top -- being the so-called -- it accumulates and the source drains 31 and 32 are formed That is, it accumulates and the source drains 31 and 32 consist of the source drain 14, silicon epitaxial layers 33 and 34 currently formed on 15, and refractory-metal silicide layers 35 and 36 currently formed in the silicon epitaxial layers 33 and 34. In addition, the offset insulator layer 16 is formed on the gate electrode 13, and the sidewall insulator layers 17 and 18 are formed in the side attachment wall of this gate electrode 13. Moreover, the above-mentioned source drains 14 and 15 are good for the sidewall insulator layer 17 and the strain effect silicon layer 24 under 18 also as LDD structure in which the low concentration diffusion layer was formed.

[0057] the field-effect transistor 3 which, on the other hand, explained the field-effect transistor 4 by drawing 5 -- setting -- source drain 74 and 75 top -- being the so-called -- it accumulates and the source drains 81 and 82 are formed That is, it accumulates and the source drains 81 and 82 consist of the source drain 74, silicon epitaxial layers 83 and 84 currently formed on 75, and refractory-metal silicide layers 85 and 86 currently formed in the silicon epitaxial layers 83 and 84. In addition, the offset insulator layer 76 is formed on the gate electrode 73, and the sidewall insulator layers 77 and 78 are formed in the side attachment wall of this gate electrode 73. Moreover, th above-mentioned source drains 74 and 75 are good for the sidewall insulator layer 77 and the strain effect silicon layer 24 under

78 also as LDD structur in which the low concentration diffusion layer was formed. Moreover, the gate electrodes 13 and 73 may be formed with polycide structure. With this polycide structure, the above-mentioned offset insulator layers 16 and 76 are not formed.

[0058] Without accumulating and silicide-izing the source drains 14 and 15 and the source drains 74 and 75 the source drains 31 and 32 and by having accumulated and having formed the source drains 81 and 82, the above-mentioned semiconductor device 5 enables it to reduce sheet resistance of the source drains 14 and 15 and the source drains 74 and 75, where shallow junction is maintained. Consequently, the high-speed operation of the wiring connected to the source drains 14 and 15 and the source drains 74 and 75 becomes possible.

[0059] The manufacturing process view of drawing 7 explains an example of the 1st operation gestalt concerning the manufacture method of the semiconductor device of this invention. In drawing 7 , the same sign is given to the same component part as aforementioned drawing 5 explained.

[0060] By the same method as (1) of aforementioned drawing 3 explained, as shown in (1) of drawing 7 p which changed germanium concentration in the thickness direction on the silicon substrate 21 - The buffer layer 22 which consists of silicon germanium (Si1-x Gex) of type For example, it forms in the thickness of 1.6 micrometers by changing composition of germanium to x= 0.3 from x= 0.04 towards an upper layer side, and depositing silicon germanium from a silicon-substrate 21 side. p which was able to be pulled up by the CZ process in the above-mentioned silicon substrate 21 - A type silicon substrate is used.

[0061] n by which stress is furthermore eased on the above-mentioned buffer layer 22 - Composition of germanium deposits the silicon germanium of x= 0.3 on the thickness of about 0.6 micrometers, and forms the relaxed layer 23 which consists of silicon germanium of type. And the strain effect silicon layer 24 used as the semiconductor layer which has the strain effect is formed as an example on this relaxed layer 23 at the thickness of 13nm. the thickness in which this strain effect silicon layer 24 can pull out the strain effect, for example, the thickness of 5nm - 30nm, -- it is good if preferably formed in the thickness of 5nm - 15nm In this strain effect silicon layer 24, tensile stress has arisen by the difference in the lattice constant of a silicon germanium layer (relaxed layer 23) and a silicon layer (the strain effect silicon layer 24). Thus, the semiconductor substrate 11 is formed.

[0062] Then, it forms in the upper layer of the strain effect silicon layer 24 to the relaxed layer 23 by the formation method of the isolation field of the usual trench structure, applying the isolation field 51 of the trench structure of separating electrically the field in which the field-effect transistor 3 of the field in which the n channel type field-effect transistor 1 is formed, and a p-channel type is formed. In addition, the formation method of the isolation field of the above-mentioned usual trench structure is a method of forming the isolation field 51, by embedding an insulator layer in the trench and removing the excessive insulator layer on the semiconductor substrate 11 by etchback, chemical mechanical polishing, etc. after that, after forming a trench in the semiconductor substrate 11 with for example, lithography technology and etching technology.

[0063] subsequently, the field applied to the upper layer of the strain effect silicon layer 24 in which the n channel type field-effect transistor 1 is formed, and the relaxed layer 23 -- p -- a well 25 is formed with ion-implantation On n wells 26, for example, the resist mask (illustration abbreviation) is formed in that case. then, the field applied to the upper layer of the strain effect silicon layer 24 in which the p-channel type field-effect transistor 3 is formed, and the relaxed layer 23 after removing the above-mentioned resist mask -- n -- a well 26 is formed with ion-implantation On p wells 25, for example, the resist mask (illustration abbreviation) is formed in that case. And this resist mask is removed after an ion implantation. In addition, whichever the n above-mentioned well 26 and p wells 25 form previously, inconvenience does not have them. Hereafter, in (2) - (4) of drawing 7 , illustration of a part of silicon substrate 21 and buffer layer 22 is omitted.

[0064] Subsequently, by the same method, as shown in (2) of drawing 7 , the gate insulator lay r 12 (72) is formed by the silicon oxide on the strain effect silicon layer 24 as (2) of aforementioned drawing 3 explained. Then, after depositing contest polysilicon and forming the gat electrode layer 41 (portion shown according to a two-dot chain line) by CVD, With the etching technology which carried out patterning of the resist film with formation of the resist film (illustration abbreviation) by resist application, and lithography technology, and used formation of a resist mask (illustration abbreviation),

and its resist mask for the etching mask While forming the gate electrode 13 of an n channel type field-effect transistor which consists of a gate electrode layer 41 on the gate insulator layer 12, the gate electrode 73 of a p-channel type field-effect transistor which consists of a gate lectrode layer 41 is formed on the gate insulator layer 72. By this etching, the portion shown according to the two-dot chain line of the gate insulator layer 12 (72) also **********s.

[0065] Subsequently, as shown in (3) of drawing 7 , after forming a wrap resist mask (illustration ellipsis) for the p well 25 top with a resist application and lithography technology, the ion implantation of the p type impurity for forming the source drain of a p-channel type field-effect transistor is carried out. in this ion implantation, the gate electrode 73 is used as a mask, the ion implantation for example, of the 2 boron-fluoride ion (BF2+) is carried out to the strain effect silicon layer 24 in the both sides of the gate electrode 73 as the above-mentioned p type impurity, and the source drains 74 and 75 of n mold are formed in the upper layer of the strain effect silicon layer 24 As the above-mentioned ion-implantation conditions, when 2 boron-fluoride ion (BF2+) is used for p type impurity, the projection range of 2 boron-fluoride ion is set as 5nm by setting placing energy to 5keV(s), and it is a dose 3x1015 pieces/cm, for example, 2 It set up. Then, for example, oxygen ashing and washing processing remove the above-mentioned resist mask. In addition, a thin oxide film (illustration ellipsis) may be formed before the ion implantation of the above-mentioned boron, and this thin oxide film may be removed after the ion implantation.

[0066] Then, as shown in (4) of drawing 7 , after forming a wrap resist mask (illustration ellipsis) for the n well 26 top with a resist application and lithography technology, the ion implantation of the n type impurity for forming the source drain of an n channel type field-effect transistor is carried out. in this ion implantation, the gate electrode 13 is used as a mask, the ion implantation of the arsenic ion (As+) is carried out to the strain effect silicon layer 24 in the both sides of the gate electrode 13 as the above-mentioned n type impurity, and the source drains 14 and 15 of n mold are formed in the upper layer of the strain effect silicon layer 24 As the above-mentioned ion-implantation conditions, when arsenic ion (As+) is used for n type impurity, the projection range of arsenic ion is set as 6nm for placing energy as 5keV(s), for example, and it is a dose 5x1015 pieces/cm 2 It set up.

[0067] Subsequently, for example, oxygen ashing and washing processing remove the above-mentioned resist mask. Then, activation annealing is performed. As this annealing condition, in the case of furnace annealing, for example, annealing temperature is set up as 800 degrees C, and annealing time is set up in 30 minutes. Moreover, in the case of rapid heating annealing [ELA (Excimer Laser Annealing)], it is the energy of an irradiation laser beam 1 J/cm2 It sets up. By performing such activation annealing, the source drains 14 and 15 of shallow junction are formed. Simultaneously, the source drains 74 and 75 are also activated by this activation annealing. Thus, the semiconductor device 5 which consists of an n channel field-effect transistor 1 and a p-channel field-effect transistor 3 is formed.

[0068] In addition, although the above-mentioned source drains 14 and 15 and the source drains 74 and 75 were formed with the ion implantation, it is also possible to form, for example using methods, such as laser doping, gaseous-phase doping, and solid phase doping.

[0069] By the manufacture method of the above-mentioned semiconductor device, since the source drains 14 and 15 of the n channel field-effect transistor 1 and the source drains 74 and 75 of the p-channel field-effect transistor 3 are formed only in the strain effect silicon layer 24, each junction of the source drains 14 and 15 and the source drains 74 and 75 will be formed only in the strain effect silicon layer 24. Therefore, generating of junction leak is suppressed. Moreover, since each source drains 14 and 15 and the source drains 74 and 75 are formed in the one strain effect silicon layer 24 and it is not necessary to manufacture the channel cambium corresponding to each source drains 14 and 15 and the source drains 74 and 75, a manufacture process becomes easy.

[0070] Next, the manufacturing process view of drawing 8 explains an example of the 2nd operation gestalt concerning the manufacture method of a semiconductor device below. In drawing 8 , the same sign is given to the same thing as the component part shown in aforementioned drawing 4 and drawing 6 .

[0071] In the manufacture method of the semiconductor device explained by aforementioned drawing 7 , after forming the gate electrode layer 41 and forming the offset insulator layer 16 on the gate insulator

layer (41) used as the gate electrodes 13 and 73 as shown in (1) of drawing 8 , patterning of the gate is perform d. Subsequently, the source drains 14 and 15 and the source drains 74 and 75 are formed, and the sidewall insulator layers 17 and 18 and the sidewall insulator layers 77 and 78 are formed after that. In addition, in making the above-mentioned source drains 14 and 15 and the source drains 74 and 75 into LDD (Lightly Doped Drain) structure, after performing patterning of the gate, it forms the low concentration diffusion layer which forms LDD structure with an ion implantation. In this case, LDD of a p-channel type field-effect transistor is formed by the p type low concentration diffusion layer, and LDD of an n channel type field-effect transistor is formed by the n type low concentration diffusion layer. Then, while forming the sidewall insulator layers 17 and 18 in the side attachment wall of the gate electrode 13, after forming the sidewall insulator layers 77 and 78 in the side attachment wall of the gate electrode 73, each high concentration field of the source drains 14 and 15 and the source drains 74 and 75 is formed with the impurity doping technology (for example, ion implantation) which is adapted for each.

[0072] Then, alternatively, by the epitaxial grown method, on the source drain 14 and 15, silicon is deposited alternatively and the silicon epitaxial layers 33 and 34 are formed. Simultaneously, on the source drain 74 and 75, silicon is deposited alternatively and the silicon epitaxial layers 83 and 84 are formed.

[0073] Subsequently, by the same method, as shown in (2) of drawing 8 , after forming the refractory-metal (for example, titanium) layer 37 all over the silicon epitaxial layer 33, 34, and 83 side and 84 sides, heat treatment (for example, RTA) is performed, the refractory-metal silicide (for example, titanium silicide) layers 35 and 36 are formed and accumulated on the silicon epitaxial layers 33 and 34, and the source drains 31 and 32 are formed as (2) of aforementioned drawing 4 explained. Simultaneously, the refractory-metal silicide (for example, titanium silicide) layers 85 and 86 are formed and accumulated on the silicon epitaxial layers 83 and 84, and the source drains 81 and 82 are formed. Then, etching removes the unreacted refractory-metal layer 37 (portion shown according to a two-dot chain line), for example. Thus, the semiconductor device 5 which consists of a field-effect transistor 2 which accumulated and formed the source drains 31 and 32, and a field-effect transistor 4 which accumulated and formed the source drains 81 and 82 is formed. In addition, in the above-mentioned silicide-izing, in forming the gate electrodes 13 and 73 in polycide structure simultaneously, the above-mentioned offset insulator layers 16 and 76 form the above-mentioned refractory-metal layer 37 in the gate electrode 13 and the state of contacting on 73 without forming.

[0074] By the manufacture method of the above-mentioned semiconductor device, since the upper part of the source drains 14, 15, and 74 and the silicon epitaxial layers 33, 34, 83, and 84 deposited on 75 is silicide-ized, and is accumulated and the source drains 31, 32, 81, and 82 are formed, the source drains 14, 15, 74, and 75 are not silicide-ized. For the reason, where shallow junction of the source drains 14 and 15 is maintained, it becomes possible to reduce sheet resistance of the source drains 14 and 15. Similarly, sheet resistance of the source drains 74 and 75 is also reduced.

[0075] Next, the circuit diagram of drawing 9 explains an example of the 1st operation gestalt concerning the logical circuit of this invention. The following explanation attaches and explains the same sign to a thing like each component part explained by aforementioned drawing 1 and drawing 5 .

[0076] The logical circuit 111 shown in drawing 9 is ISSCC Dig.Tech.Papers and "Cascode Voltage Switch Logic:A Differential CMOS Logic Family". [Feb.] (1984) Heller, L.G.and Griffin, W.R., p16-17 It is equivalent to the circuitry currently indicated. And the n channel type field-effect transistors (nMOS) 112-115 which constitute logic, and the p-channel type field-effect transistor (pMOS) 121,122 which constitutes a pMOS intersection latch are formed in the strain effect silicon layer 24 formed in the upper layer of the semiconductor substrate 11 explained by aforementioned drawing 1 and drawing 5 . This composition is the feature of the logical circuit of this invention. That is, each source drain (illustration ellipsis) of the abov 112-nMOS 115 is also formed only in the strain effect silicon layer 24, and each source drain (illustration ellipsis) of the above pMOS121,122 is formed only in the strain effect silicon layer 24.

[0077] In the above-mentioned logical circuit 111, since each source drain of nMOS 112-115 is formed only in the strain effect silicon layer 24, junction of each source drain will exist in the strain effect silicon layer 24. Therefore, since generating of junction leak stops being able to occur easily, improvement in

the reliability of a logical circuit 111 can be aimed at. Moreover, in the above-mentioned logical circuit 111, logic consists of nMOS(s) 112-115, and the load is formed by the intersection latch of pMOS121,122. In this cas , when an output changes and a pMOS intersection latch is reversed, while a direct curr nt flows to a logical circuit and change of an output is completed, a direct current will not flow. Moreover, as a feature of this logical circuit 111, the electric field built over each transistor at the time of operation are eased. Therefore, since the fall of mobility does not take place, high-speed operation becomes possible. Moreover, since the channel layer of nMOS is formed in the strain effect silicon layer 24, a silicon network receives tensile stress by the difference of a lattice constant with the relaxed layer 23 which consists of silicon and silicon germanium of a ground. Therefore, degeneracy of the bottom of a conduction band is cleared, as for an electron, the effective mass becomes small, and mobility increases near the double precision. Therefore, the mutual conductance gm as a nMOS transistor improves near the double precision. On the other hand, since high performance is not demanded at pMOS121,122, the composition in a few element number is attained. Thus, the logical circuit in which high-speed operation is possible consists of low batteries.

[0078] Next, the circuit diagram of drawing 10 explains an example of the 2nd operation gestalt concerning a logical circuit. The following explanation attaches and explains the same sign to a thing like each component part explained by aforementioned drawing 1 and drawing 5 .

[0079] The logical circuit 131 shown in drawing 10 is IEEE J.Solid-state Circuits, "A 3.8-ns CMOS 16x16-b Multiplier Using Complementary Pass-Transistor Logic, and "25. [2] (1990) Yano, K.et al., and p388-395 It is equivalent to the circuitry currently indicated and is one of the basic circuits using the pass transistor logic. That is, the logical circuit is constituted by the nMOS path transistor. And the n channel type field-effect transistors 132-135 which constitute a pass transistor logic (nMOS), CMOS inverter 143,144 and the p-channel type field-effect transistor (pMOS) 141,142 which performs compensation of an output level <A HREF="/Tokujitu/tjitemdrw.ipdl?N0000=237&N0500=1E_N/;>?=8?97: [aforementioned drawing 1 and]///&N0001=59&N0552=9&N0553=000007" It is formed in the strain effect silicon layer 24 formed in the upper layer of the semiconductor substrate 11 explained by TARGET="tjitemdrw"> drawing 5. This composition is the feature of the logical circuit of this invention. That is, each source drain (illustration ellipsis) of the above 132-nMOS 135 is also formed only in the strain effect silicon layer 24, and the source drain (illustration ellipsis) of the above pMOS141,142 and each source drain (illustration ellipsis) of CMOS inverter 143,144 are formed only in the strain effect silicon layer 24.

[0080] In the above-mentioned logical circuit 131, since each source drain of nMOS 112-115 is formed only in the strain effect silicon layer 24, junction of each source drain will exist in the strain effect silicon layer 24. Therefore, since generating of junction leak stops being able to occur easily, improvement in the reliability of a logical circuit 111 can be aimed at. Moreover, logic is constituted by the nMOS path transistor, and it has the driving force of a load reinforced in the above-mentioned logical circuit 131, for example while "H" level returns that only the threshold voltage of nMOS falls rather than VDD with CMOS inverter 143,144 formed in the output, when it lets the signal of "H" level pass for example, to a nMOS path transistor. Furthermore, an output level is compensated by the intersection latch of pMOS141,142. That is, "H" level is amended to VDD. Driving force is not needed for pMOS141,142 for that. In addition, what is necessary is to be large in the channel width of pMOS141,142, and just to design channel length small, in order to make it reversal operation of an intersection latch of pMOS141,142 not become slow.

[0081] Subsequently, the circuit diagram of drawing 11 explains an example of the 3rd operation gestalt concerning a logical circuit. The following explanation attaches and explains the same sign to a thing like each component part explained by aforementioned drawing 1 and drawing 5 .

[0082] The logical circuit 151 shown in drawing 11 Proc.IEEE 1994 CICC and "A High Speed and LowPower, Swing Restored Pass-Transistor Logic Based Multiply and Accumulate Circuit for Multimedia Applications and" [May.] (1994) Prameswer, A., Hara, H., and Sakurai, T., and p358-362 It is equivalent to the circuitry currently indicated and is one of the basic circuits using the pass transistor logic. That is, the nMOS pass transistor logic and the CMOS latch are used. And the n channel type field-effect transistors (nMOS) 152-155 which constitute a pass transistor logic, and the p-channel type field-effect transistor (pMOS) 161,162 which constitutes a CMOS latch and th n channel type field-

effect transistor (nMOS) 163,164 are formed in the strain effect silicon layer 24 formed in the upper layer of the semiconductor substrate 11 explained by aforementioned drawing 1 and drawing 5 . This composition is th feature of the logical circuit of this invention. That is, each source drain (illustration ellipsis) of th above [nMOS / nMOS and / 163,164] 152-155 is also formed only in the strain effect silicon layer 24, and each source drain (illustration ellipsis) of the above pMOS161,162 is formed only in the strain effect silicon layer 24.

[0083] In the above-mentioned logical circuit 151, since each source drain of nMOS 112-115 is formed only in the strain effect silicon layer 24, junction of each source drain will exist in the strain effect silicon layer 24. Therefore, since generating of junction leak stops being able to occur easily, improvement in the reliability of a logical circuit 131 can be aimed at.

[0084] Furthermore, since a CMOS latch has the feature to which a margin of operation becomes large as compared with a pMOS intersection latch in order to operate with a push pull and static current does not flow, a working speed becomes quick. Therefore, rather than the aforementioned logical circuit 131, low-power-ization can be attained and high-speed operation becomes possible. Moreover, even if the ratio of each gate width of pMOS of the CMOS latch to the path transistor of nMOS composition and nMOS changes, it has the advantage which can take the large optimal field of a time delay. Therefore, the design margin has the advantage to which it becomes large and a manufacture margin also becomes large in connection with it.

[0085] In addition, the above-mentioned logical circuit 111,131,151 is an example, and it is possible to use the composition which forms a field-effect transistor 1 and a semiconductor device 5 for the strain effect silicon layer 24 explained to other logical circuits using the path transistor network, for example, DSL, (Differential Split-Level logic), DCVSPG (Differential Cascode Voltage Switch with the Pass-Gate), etc. by above-mentioned drawing 1 , drawing 5 , etc.

[0086] Next, the outline composition cross section of drawing 12 explains an example of the operation gestalt concerning the semiconductor substrate of this invention. In drawing 12 , the same sign is given to the same thing as the component part explained by aforementioned drawing 1 .

[0087] As shown in drawing 12 , as for the semiconductor substrate 91, the strain effect silicon layer 24 which is a semiconductor layer in which the relaxed layer 23 is formed in and has the strain effect at a it top is formed on the germanium substrate 92. The above-mentioned relaxed layer 23 is n. - It consists of silicon germanium (Si0.7 germanium0.3) with which the stress of type (or p-) is eased, for example, is formed in the thickness of about 0.6 micrometers. In addition, the composition ratio of germanium is not limited to the above-mentioned value, and is chosen suitably. Moreover, the strain effect silicon layer 24 is the same as that of what was explained by aforementioned drawing 1 . The semiconductor substrate 91 is constituted like the above.

[0088] In the above-mentioned semiconductor substrate 91, since the germanium substrate 92 is us d, it is possible to form the relaxed layer 23 which consists of a silicon germanium layer by which stress is eased directly, without forming a buffer layer on the germanium substrate 92. That is, since grid mismatching cannot occur easily between the germanium substrate 92 and the relaxed layer 23, it becomes possible to adopt the above-mentioned composition. Therefore, the structure of the semiconductor substrate 91 is simplified and the process which forms this semiconductor substrate 91 is also simplified.

[0089] Next, the above-mentioned semiconductor substrate 91 can form in the strain effect silicon layer 24 of the semiconductor substrate 91 the field-effect transistor 1 explained by aforementioned drawing 1 using the semiconductor substrate 91 explained by above-mentioned drawing 12 instead of the aforementioned semiconductor substrate 11 explained by aforementioned drawing 1 . Moreover, it is also possible to form in the strain effect silicon layer 24 of the semiconductor substrate 91 the semiconductor device 5 explained by aforementioned drawing 5 using the semiconductor substrate 91 explained by above-mentioned drawing 12 instead of the aforementioned semiconductor substrate 11 explained by aforementioned drawing 5 .

[Translation done.]

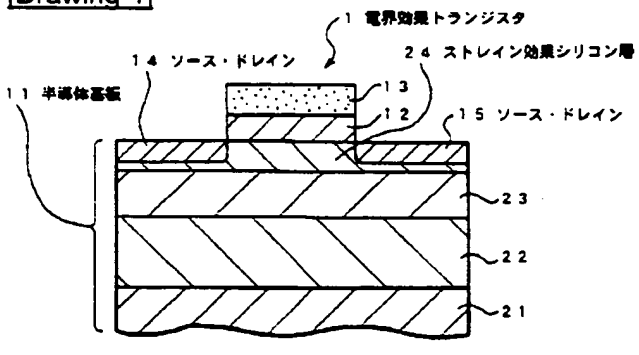
DESCRIPTION OF DRAWINGS

[Brief Description of th Drawings]
[Drawing 1] It is the outline composition cross section of the 1st operation gestalt concerning a field-effect transistor.
[Drawing 2] It is the outline composition cross section of the 2nd operation gestalt concerning a field-effect transistor.
[Drawing 3] It is the manufacturing process view of the 1st operation gestalt concerning the manufacture method of a field-effect transistor.
[Drawing 4] It is the manufacturing process view of the 2nd operation gestalt concerning the manufacture method of a field-effect transistor.
[Drawing 5] It is the outline composition cross section of the 1st operation gestalt concerning a semiconductor device.
[Drawing 6] It is the outline composition cross section of the 2nd operation gestalt concerning a semiconductor device.
[Drawing 7] It is the manufacturing process view of the 1st operation gestalt concerning the manufacture method of a semiconductor device.
[Drawing 8] It is the manufacturing process view of the 2nd operation gestalt concerning the manufacture method of a semiconductor device.
[Drawing 9] It is the circuit diagram of the 1st operation gestalt concerning a logical circuit.
[Drawing 10] It is the circuit diagram of the 2nd operation gestalt concerning a logical circuit.
[Drawing 11] It is the circuit diagram of the 3rd operation gestalt concerning a logical circuit.
[Drawing 12] It is the outline composition cross section of the operation gestalt concerning a semiconductor substrate.
[Description of Notations]
1 Field-effect Transistor 11 Semiconductor Substrate
14 15 Source drain 24 Semiconductor layer which has the strain effect

[Translation done.]

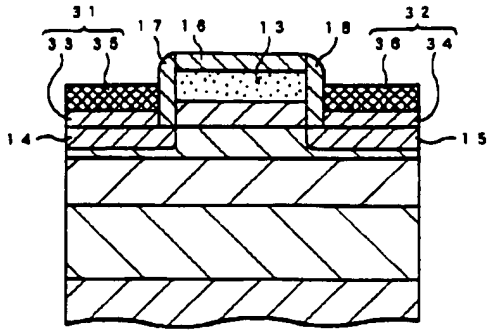
DRAWINGS

[Drawing 1]



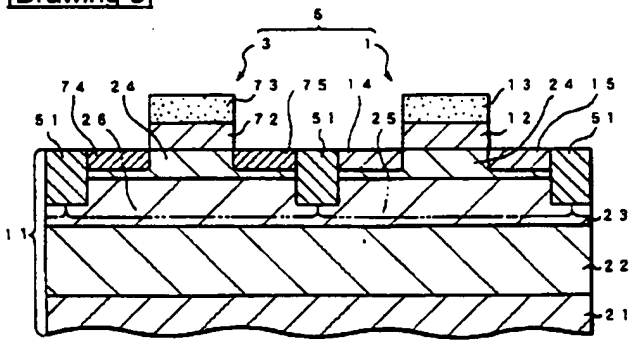
電界効果トランジスタに係わる第1実施形態の概略構成断面図

[Drawing 2]



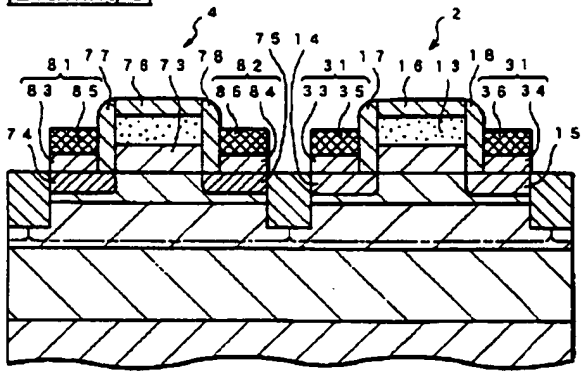
電界効果トランジスタに係わる第２実施形態の概略構成断面図

[Drawing 5]



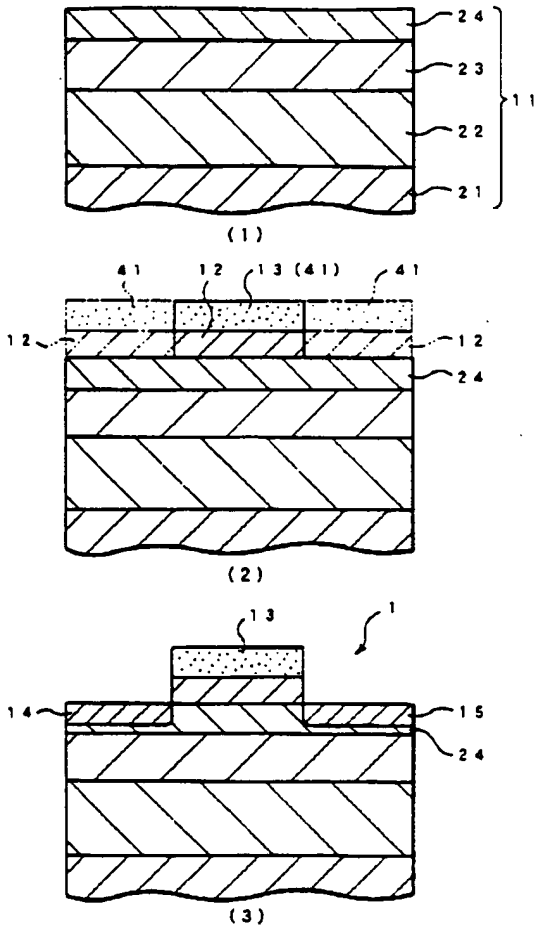
半導体装置に係わる第１実施形態の概略構成断面図

[Drawing 6]



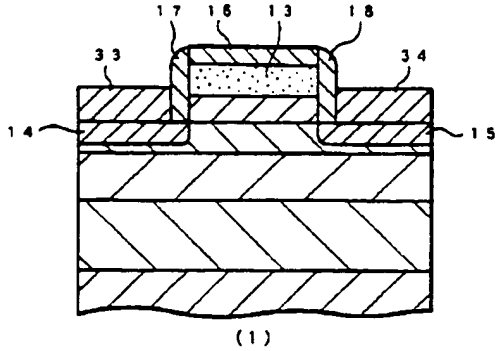
半導体装置に係わる第２実施形態の概略構成断面図

[Drawing 3]

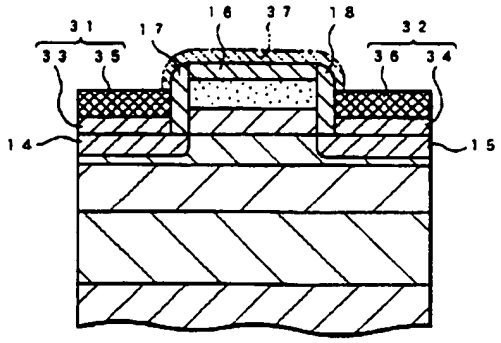


電界効果トランジスタの製造方法に係わる第１実施形態の製造工程図

[Drawing 4]



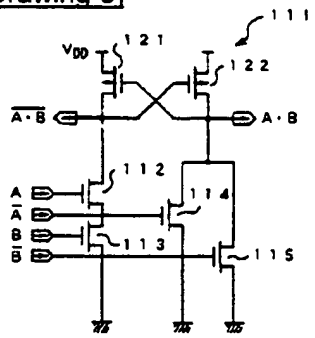
(1)



(2)

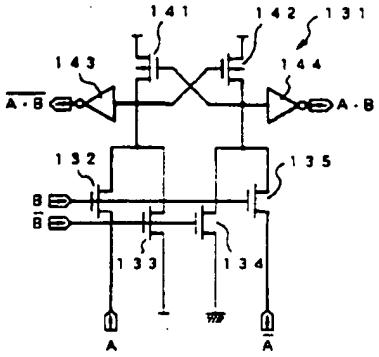
電界効果トランジスタの製造方法に係わる第２実施形態の製造工程図

[Drawing 9]



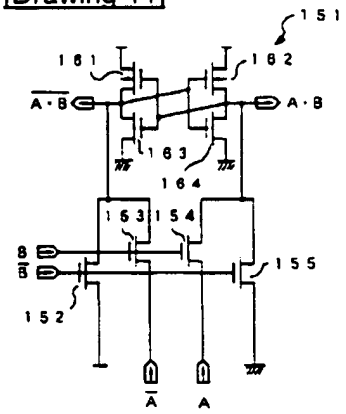
論理回路に係わる第１実施形態の回路図

[Drawing 10]



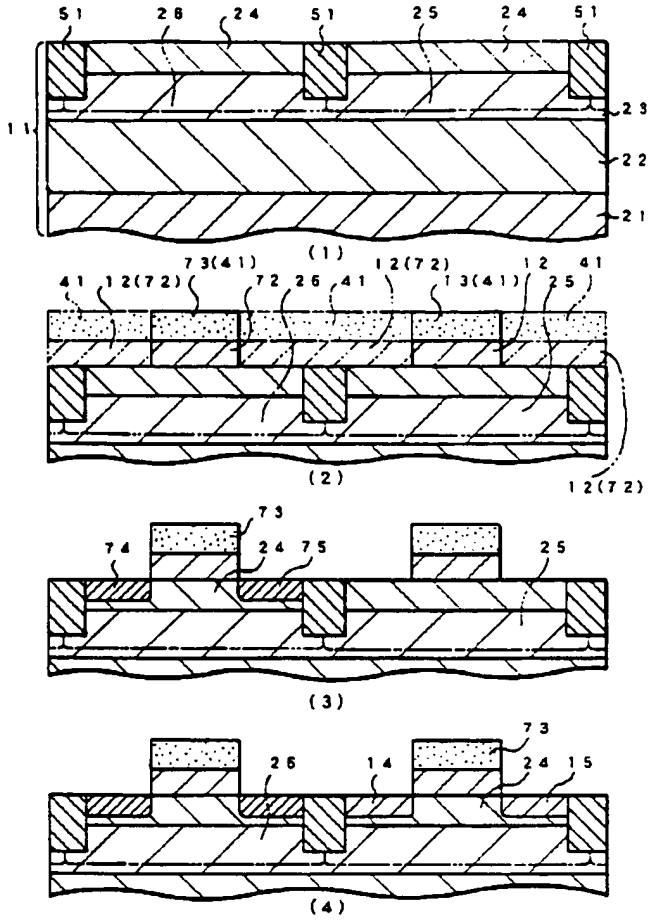
論理回路に係わる第２実施形態の回路図

[Drawing 11]



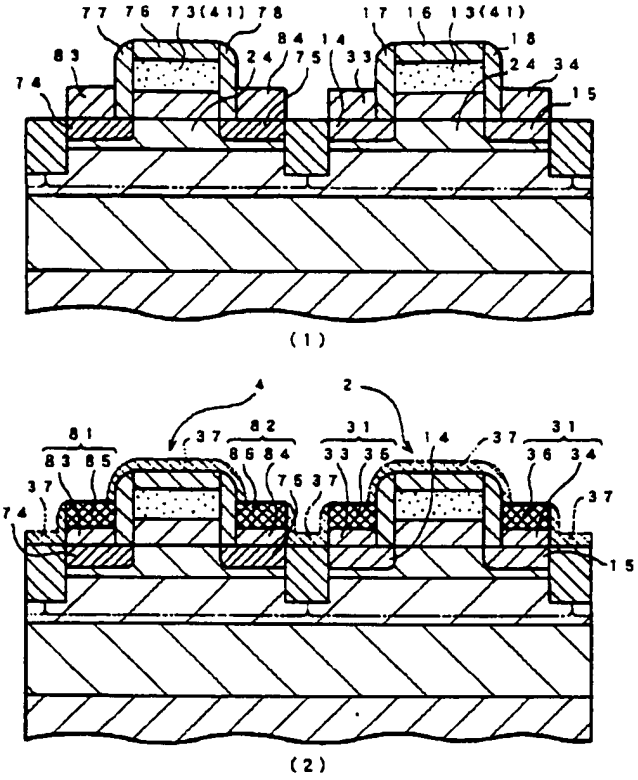
論理回路に係わる第３実施形態の回路図

[Drawing 7]



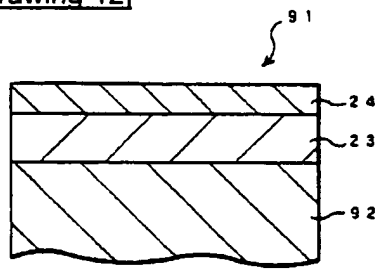
半導体装置の製造方法に係わる第１実施形態の製造工程図

[Drawing 8]



半導体装置の製造方法に係わる第２実施形態の製造工程図

[Drawing 12]



半導体基板に係わる実施形態の概略構成断面図

[Translation done.]